

# PG132-A02

370W, FH Std PCB, 384b, GDDR6x 2CH X16  
DP + DP + DP + HDMI/DP

## TABLE OF CONTENTS

Page Description

Page Description

V389-20

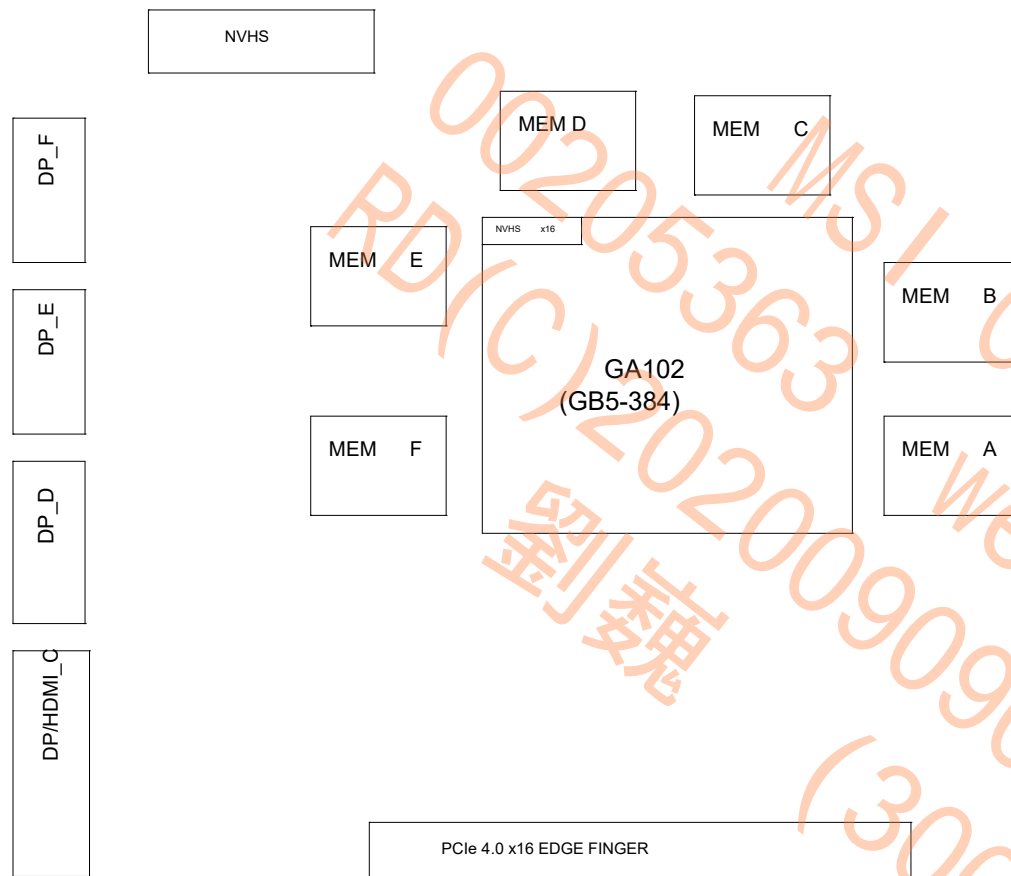
Page Description

1	Table of Contents
2	BLOCK DIAGRAM
3	PCI EXPRESS
4	MEMORY: GPU PARTITION A/B
5	MEMORY: FBA PARTITION[31:0]
6	MEMORY: FBA PARTITION[63:32]
7	MEMORY: FBB PARTITION[31:0]
8	MEMORY: FBB PARTITION[63:32]
9	MEMORY: GPU PARTITION C/D
10	MEMORY: FBC PARTITION[31:0]
11	MEMORY: FBC PARTITION[63:32]
12	MEMORY: FBD PARTITION[31:0]
13	MEMORY: FBD PARTITION[63:32]
14	MEMORY: GPU PARTITION E/F
15	MEMORY: FBE PARTITION[31:0]
16	MEMORY: FBE PARTITION[63:32]
17	MEMORY: FBF PARTITION[31:0]
18	MEMORY: FBF PARTITION[63:32]
19	GPU GND, RFUs & RSVD
20	GPU POWERS
21	GPU DECOUPLING NVVDD
22	GPU DECOUPLING FBVDDQ
23	GPU DECOUPLING MSVDD
24	BLANK
25	NVHS x16
26	MISC: THERMAL, JTAG, GPIO
27	IFPA UNUSED, IFPB UNUSED
28	IFPE DP
29	IFPD DP
30	IFPC HDMI/DP
31	IFPF DP
32	MISC. ROM, STRAPS
33	MISC. XTAL, PLL
34	PS: 5V
35	PS: PEX_DVDD and 1V8
36	BLANK
37	PS: FBVDD Controller OVR3
38	PS: FBVDDQ OVR4

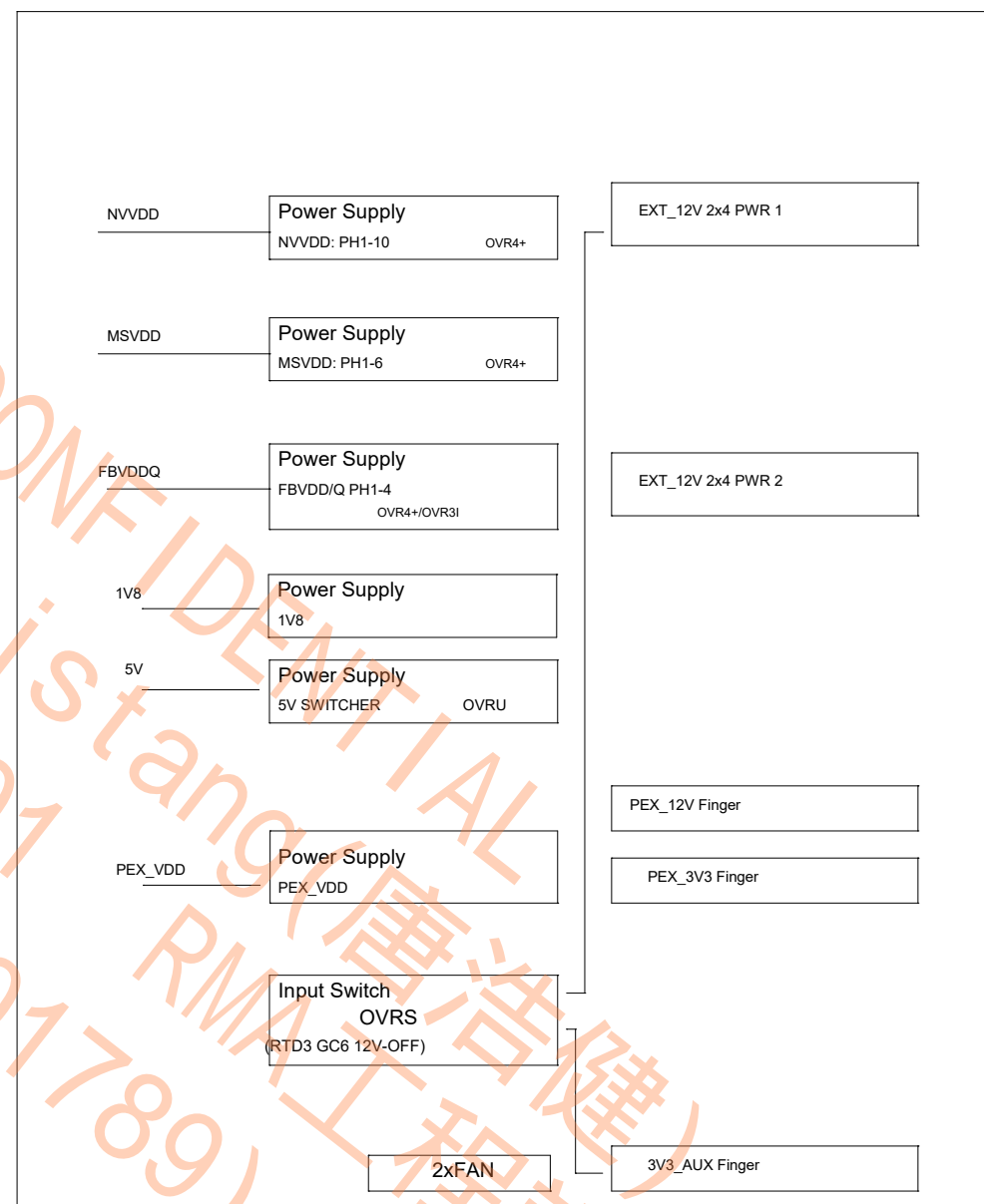
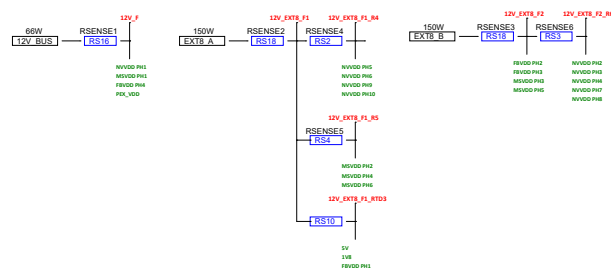
39	PS: FBVDD PH1
40	PS: FBVDD PH3
41	PS: FBVDD PH2
42	PS: FBVDD PH4
43	PS: FBVDD OUTPUT CAP
44	PS: FBVDD_OUTPUT_CAP_NEAR_MEMORY
45	PS: MSVDD CONTROLLER
46	PS: MSVDD PH1
47	PS: MSVDD PH2
48	PS: MSVDD PH3 and PH5
49	PS: MSVDD PH4 and PH6
50	PS: MSVDD OUTPUT CAP(TOP)
51	BLANK
52	PS: NVVDD Controller_OVR8
53	PS: NVVDD PH1 (PWM1)
54	PS: NVVDD PH2(PWM6)
55	PS: NVVDD PH3 (PWM3) and PH4 (PWM3)
56	PS: NVVDD PH5(PWM7) and PH7(PWM8)
57	PS: NVVDD PH6 (PWM7)
58	PS: NVVDD PH8(PWM5) and PH9(PWM2)
59	PS: NVVDD PH10 (PWM4)
60	Colayout_Notes
61	BLANK
62	PS: NVVDD OUTPUT CAP(TOP)
63	BLANK
64	PS: INPUT SWITCH RTD3
65	BLANK
66	PS: INPUTS, FILTERING, and, MONITORING
67	PS: HOT UNPLUG
68	PS: Discrete Power Steering
69	PS: PREFILTER
70	PS: PREFILTER B
71	Sequence: 5V, 1V8, 3V3_SEQ
72	Sequence: NV, PEX, FB EN
73	Sequence: 3V3 MONITOR
74	Sequence: MISC
75	MISC: LED & FAN

26	Add I2CB & Remove GPIO5/11/19/31/35
32	Add Dual-BIOS
34	Remove choke co-lay & change footprint
	Add 5V_LED
35	Remove choke co-lay & change footprint
37	Remove FBVDDQ OVR3
39	Remove choke co-lay & change footprint
40	Remove choke co-lay & change footprint
	Change 12Vin source
41	Remove choke co-lay & change footprint
	Change 12Vin source
42	Remove choke co-lay & change footprint
43	Remove CAP co-lay & change footprint
46	Remove choke co-lay & change footprint
47	Remove choke co-lay & change footprint
	Change 12Vin source
48	Remove choke co-lay & change footprint
	Change 12Vin source
49	Remove choke co-lay & change footprint
	Change 12Vin source
50	Remove CAP co-lay & change footprint
53	Remove choke co-lay & change footprint
54	Remove choke co-lay & change footprint
	Change 12Vin source
55	Remove choke co-lay & change footprint
	Change 12Vin source
56	Remove choke co-lay & change footprint
	Change 12Vin source
57	Remove choke co-lay & change footprint
	Change 12Vin source
58	Remove choke co-lay & change footprint
	Change 12Vin source
62	Remove CAP co-lay & change footprint
66	Add Fuse & PEX8 INPUT3
	Change input choke footprint
67	Remove Hot Unplug Detect
68	Remove 12V CURRENT STEERING
75	Remove 2-PIN LED HEADER
76	Add MCU for LED

### Block Diagram



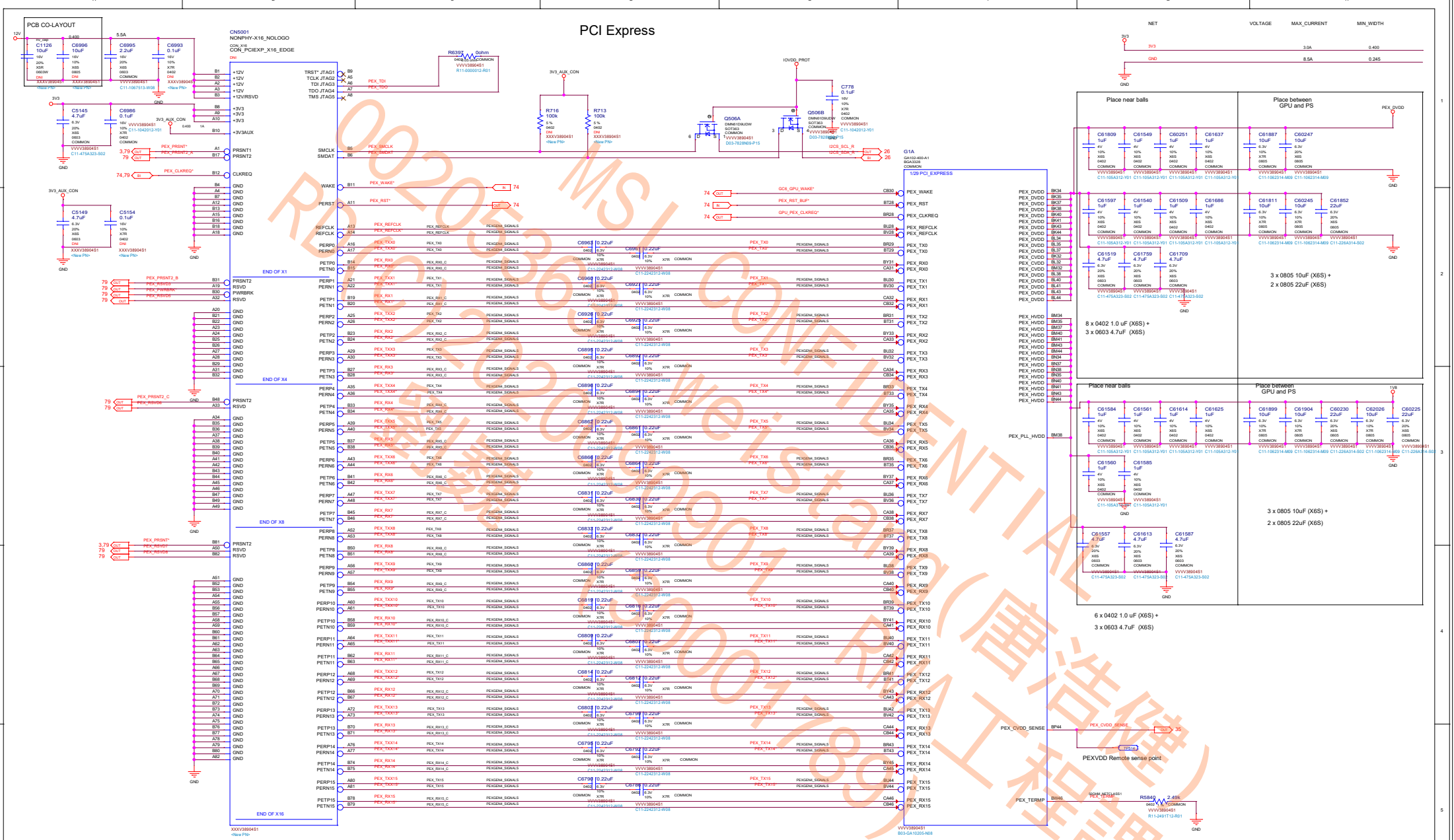
### PG132 sku30 Power Topology

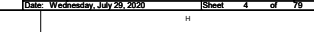


MICRO-STAR INT'L CO.-LTD

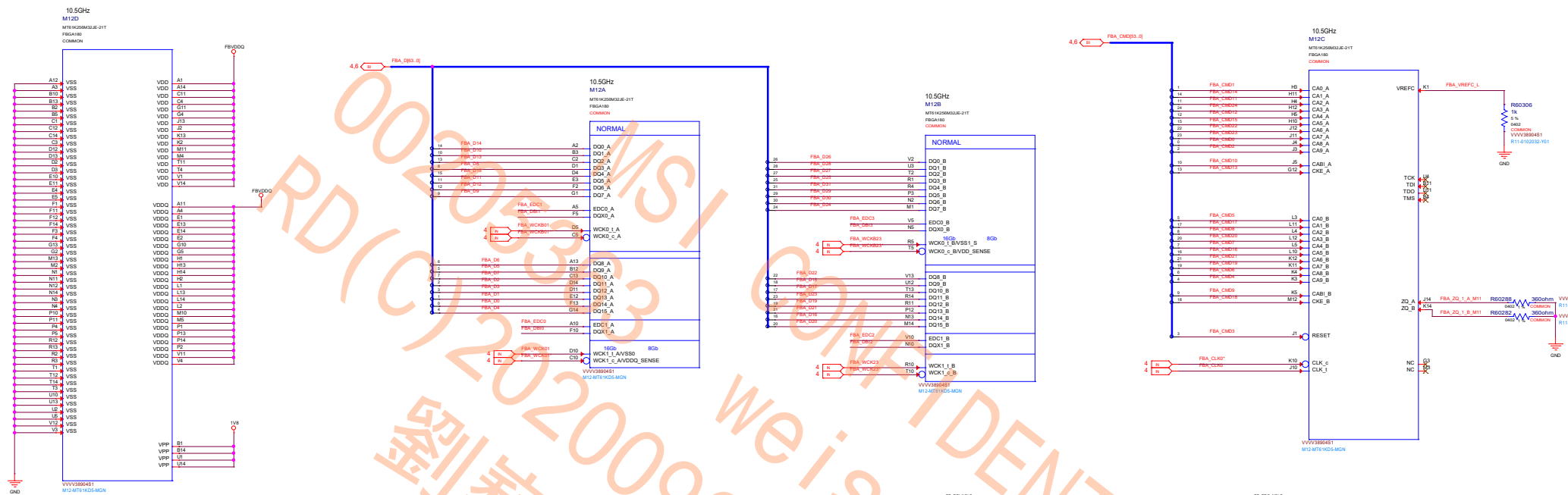
MS-V389

Size Custom	Document Description <b>BLOCK DIAGRAM</b>	Rev 2.
Date: Wednesday, July 29, 2020		Sheet 2 of 79

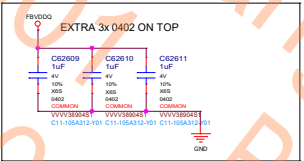




MEMORY: FBA Partition 31..0



CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



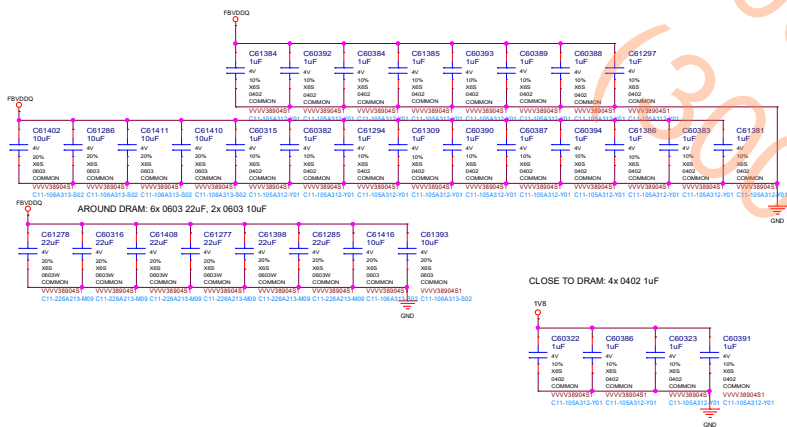
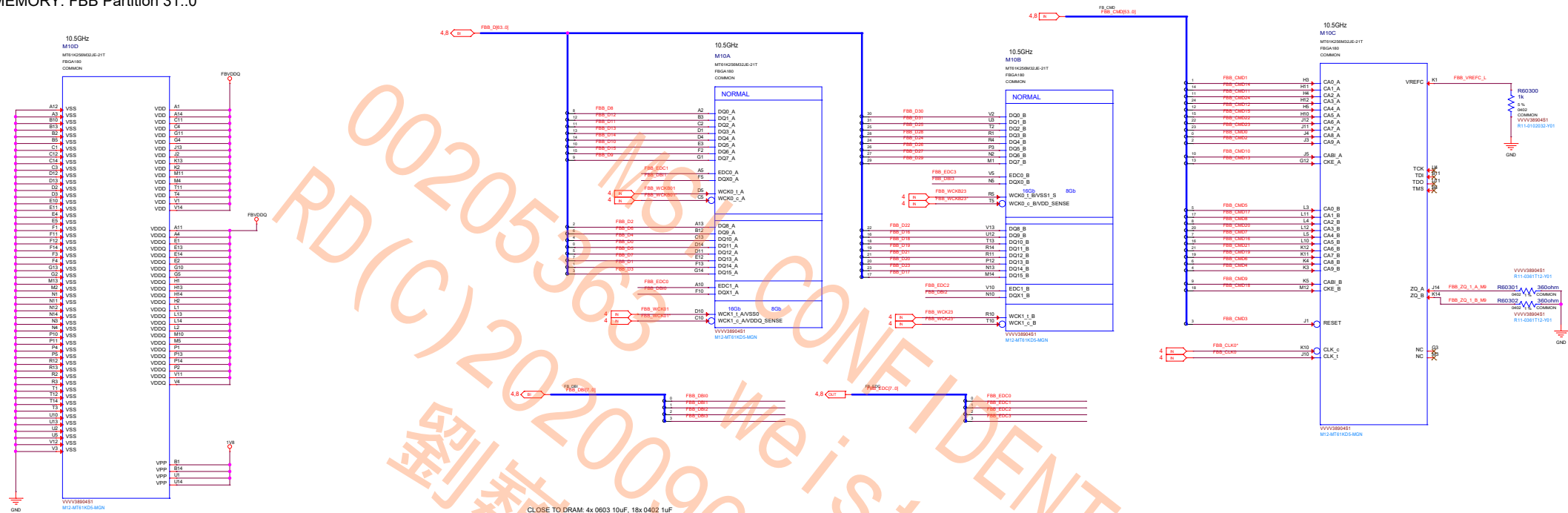
AROUND DRAM: 6x 0603 22uF, 2x 0603 10uF

CLOSE TO DRAM: 4x 0402 1uF

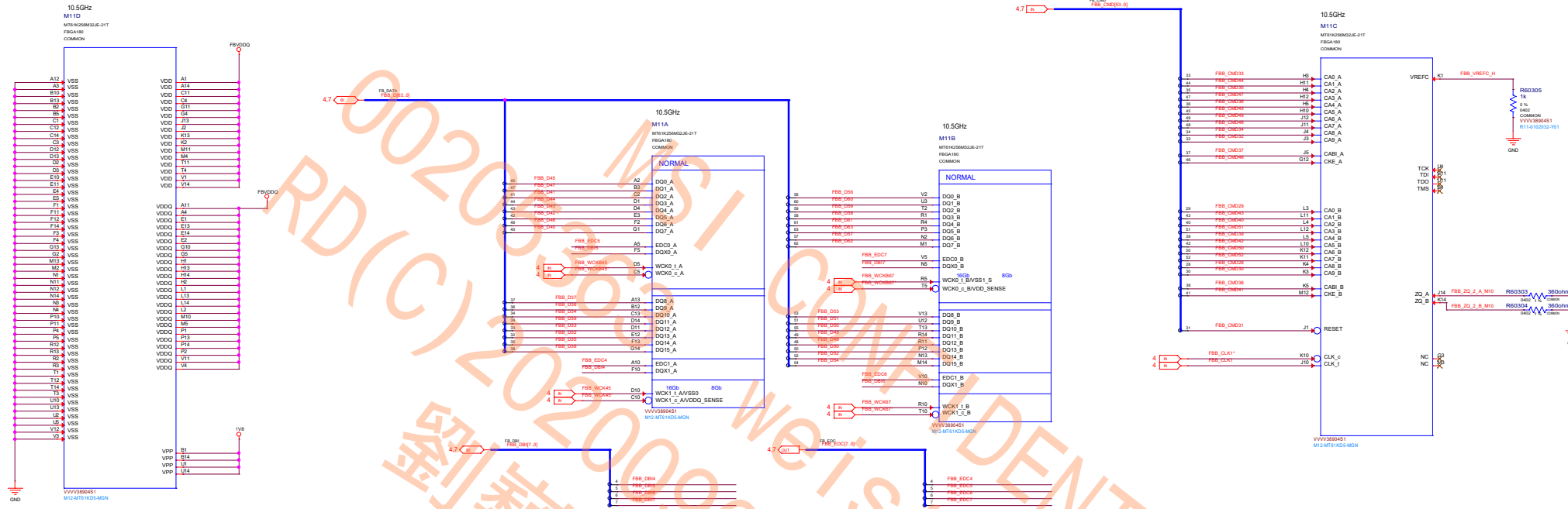




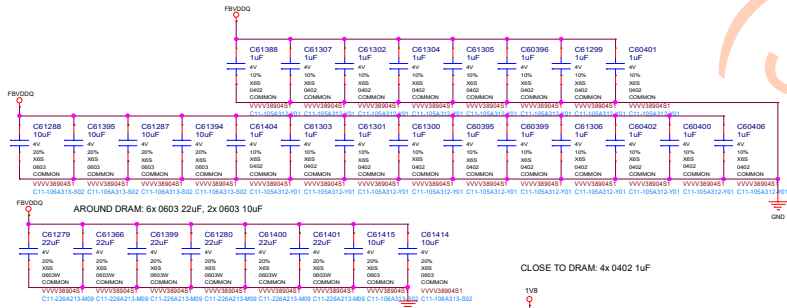
MEMORY: FBB Partition 31..0



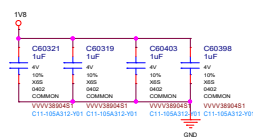
# MEMORY: FBB Partition 63..32



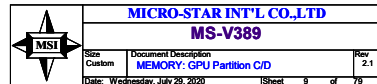
CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



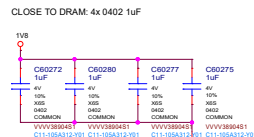
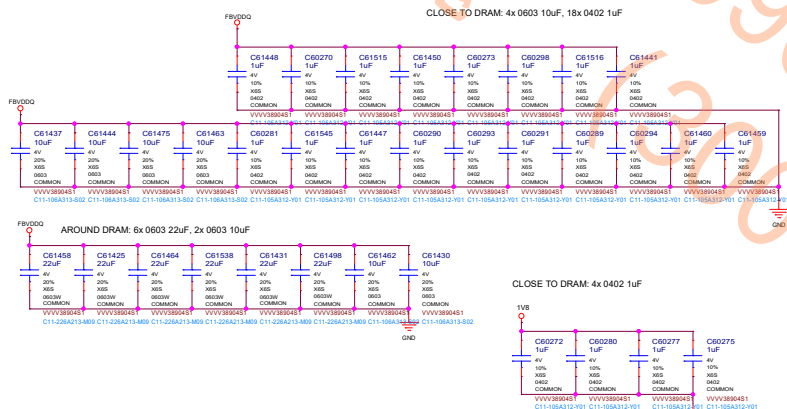
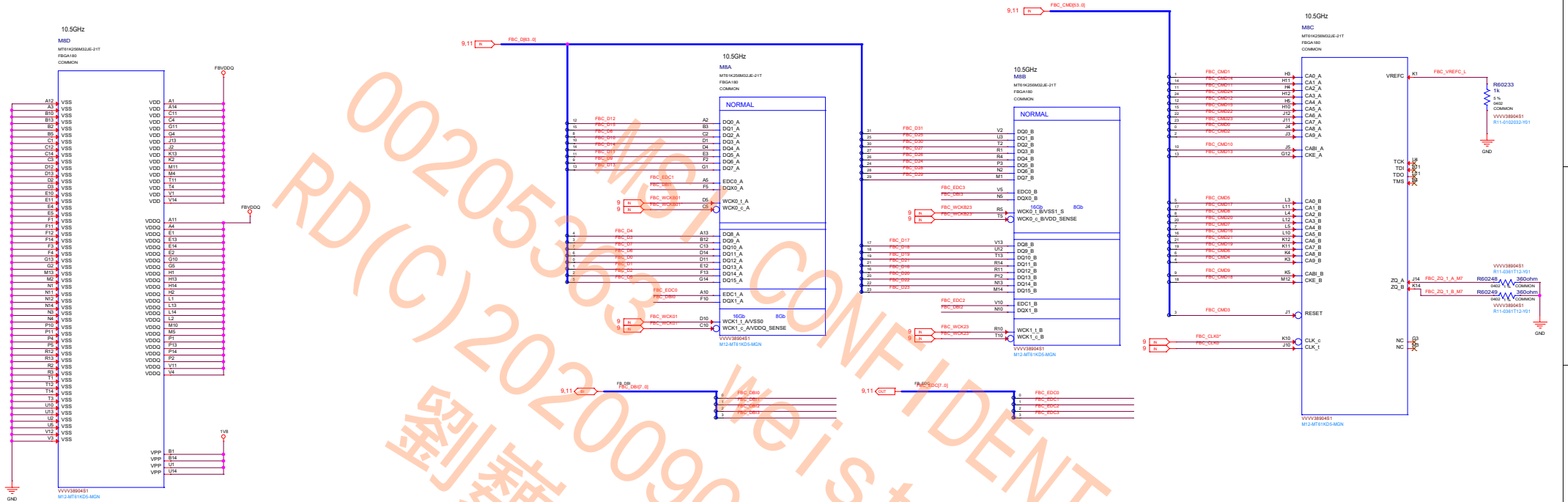
CLOSE TO DRAM: 4x 0402 1uF



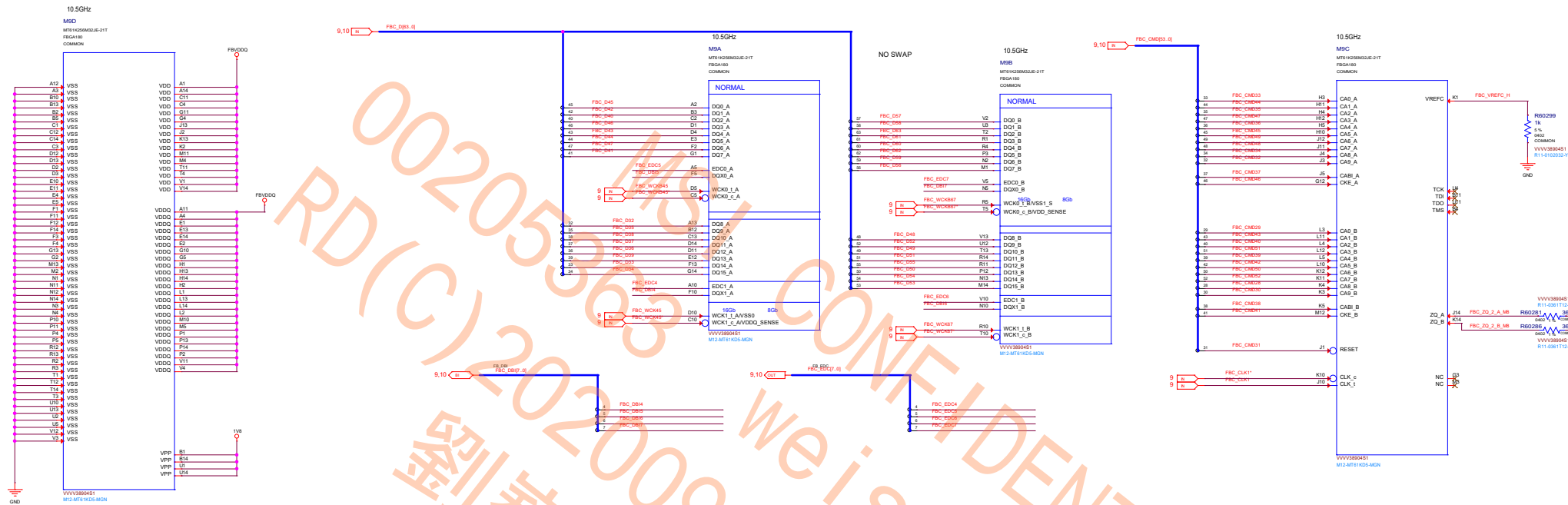




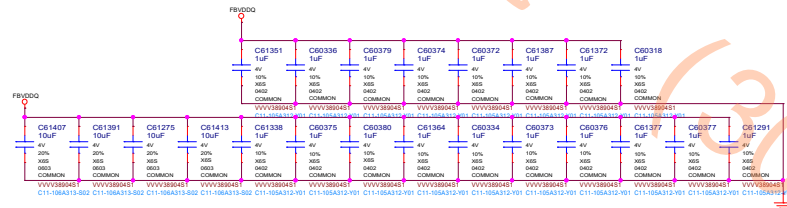
# MEMORY: FBC Partition 31..0



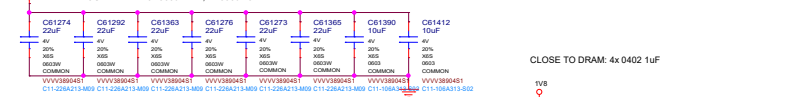
# MEMORY: FBC Partition 63..32



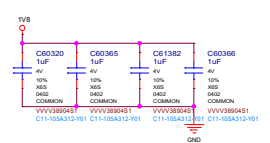
CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



AROUND DRAM: 6x 0603 22uF, 2x 0603 10uF



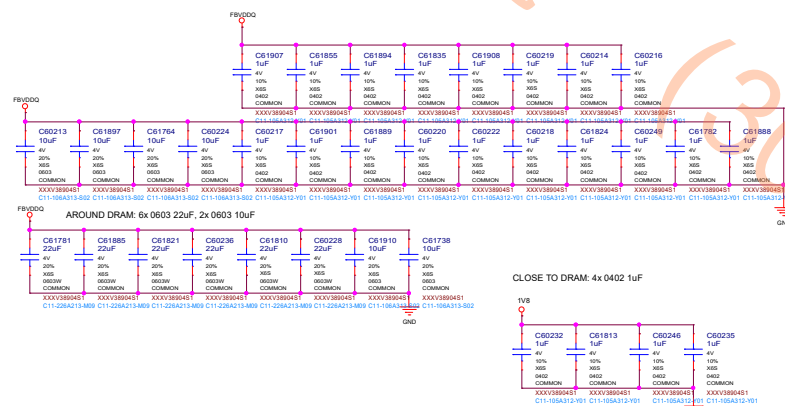
CLOSE TO DRAM: 4x 0402 1uF



MEMORY: FBD Partition 31..0

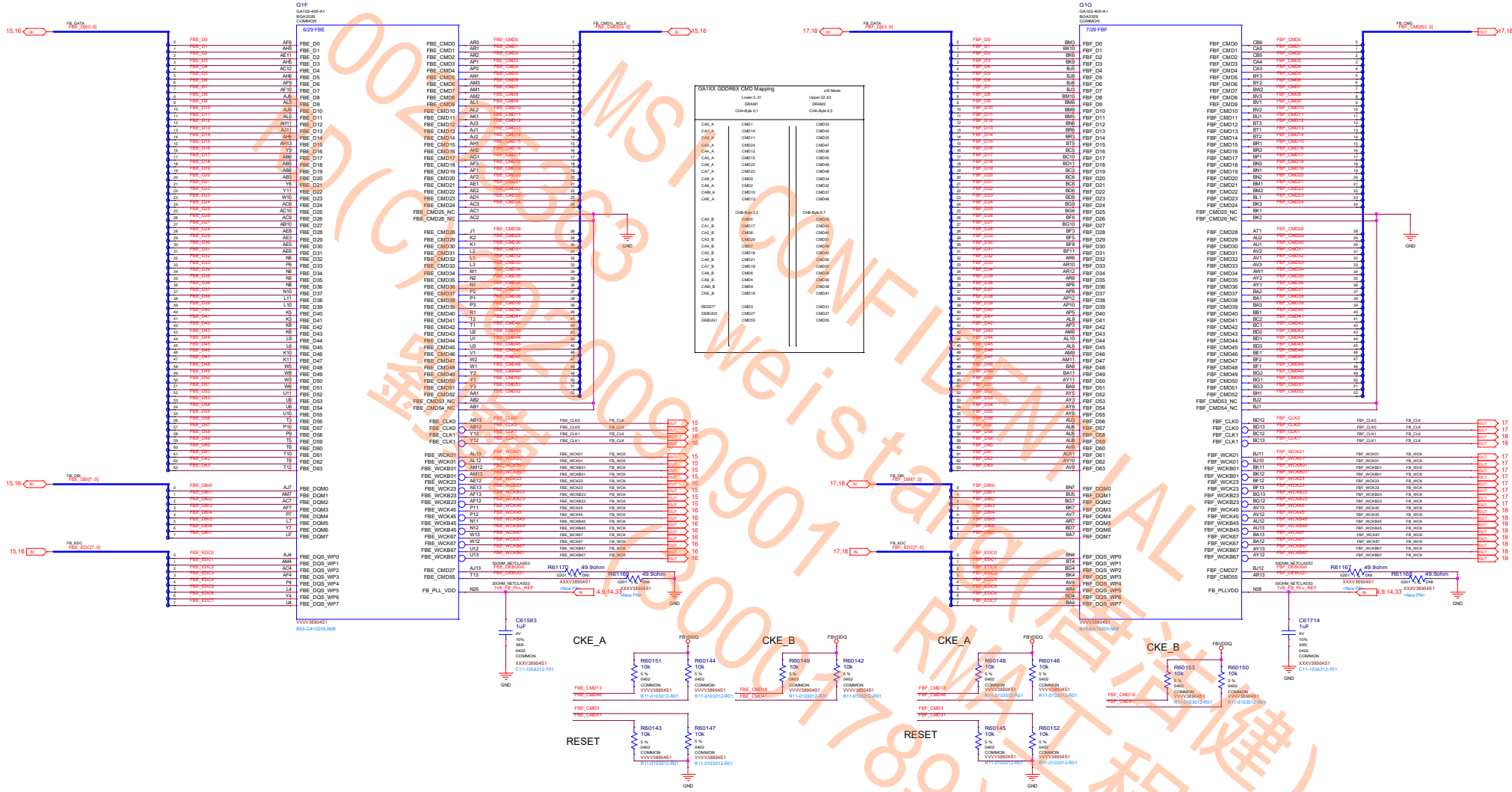


CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



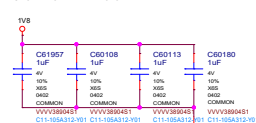
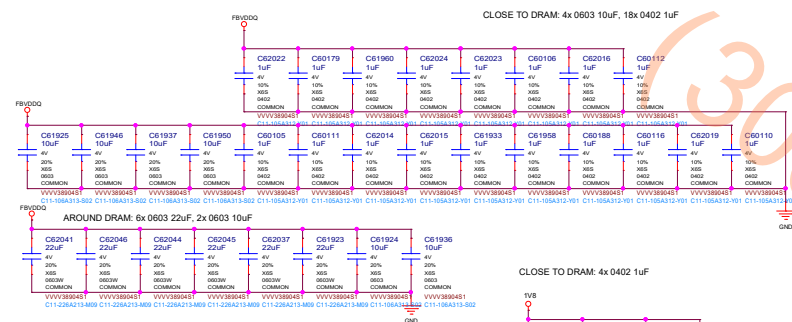
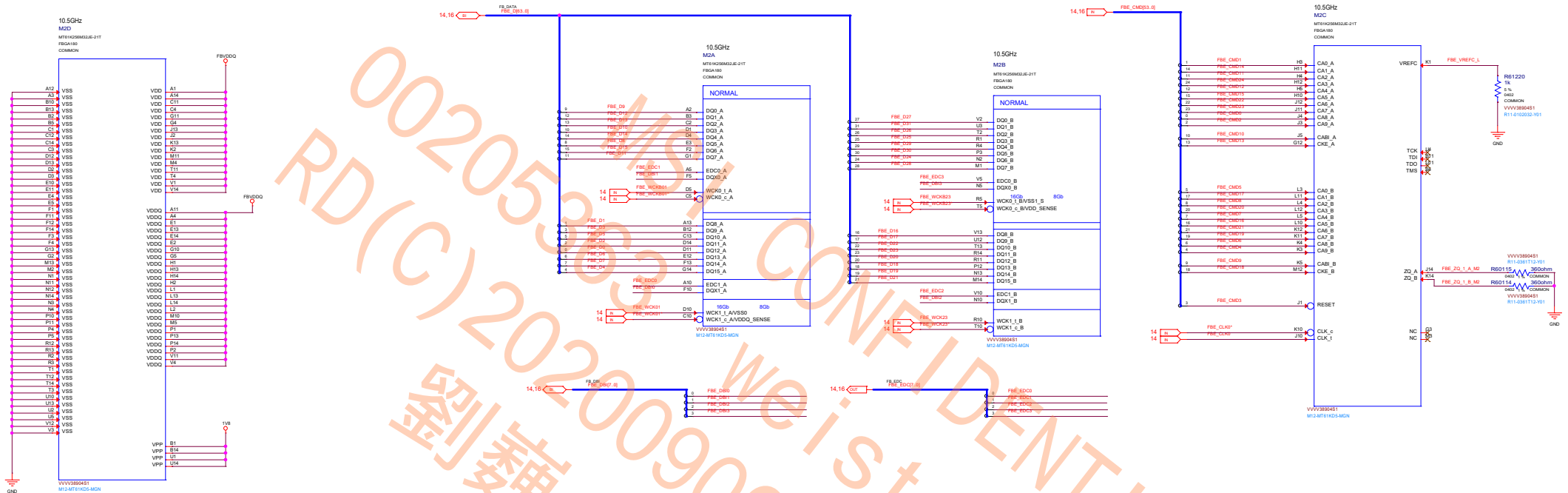
CLOSE TO DRAM: 4x 0402 1uF



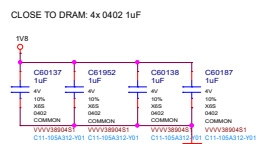
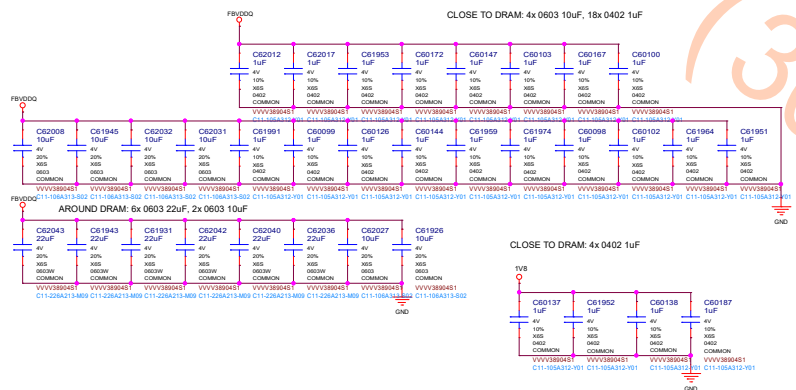
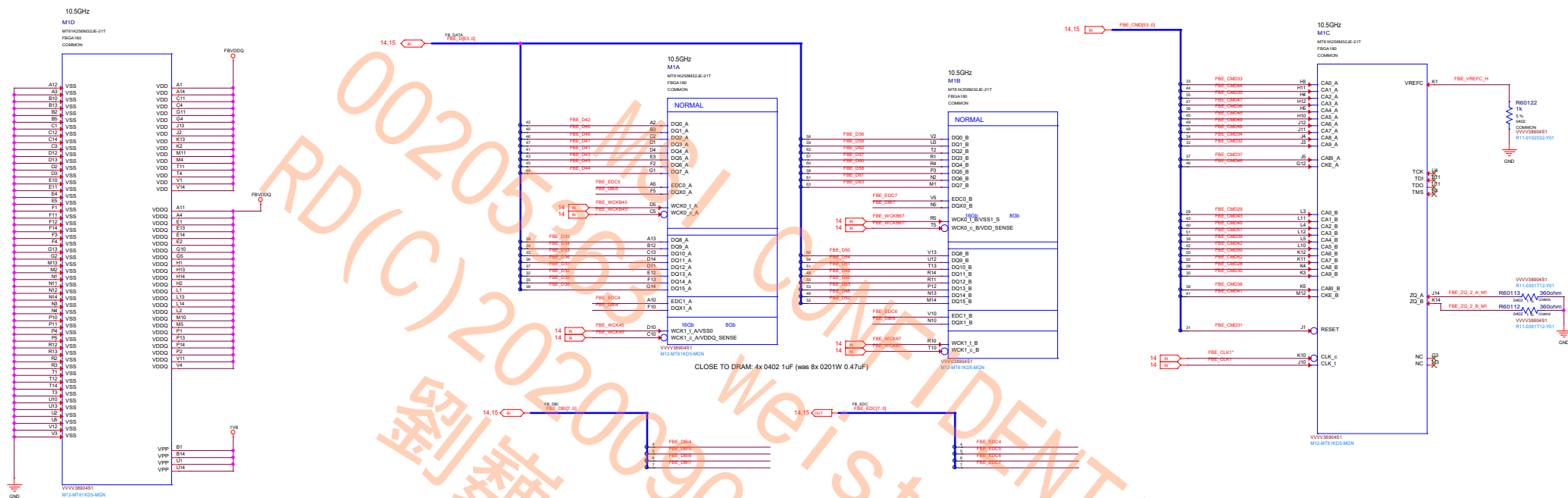




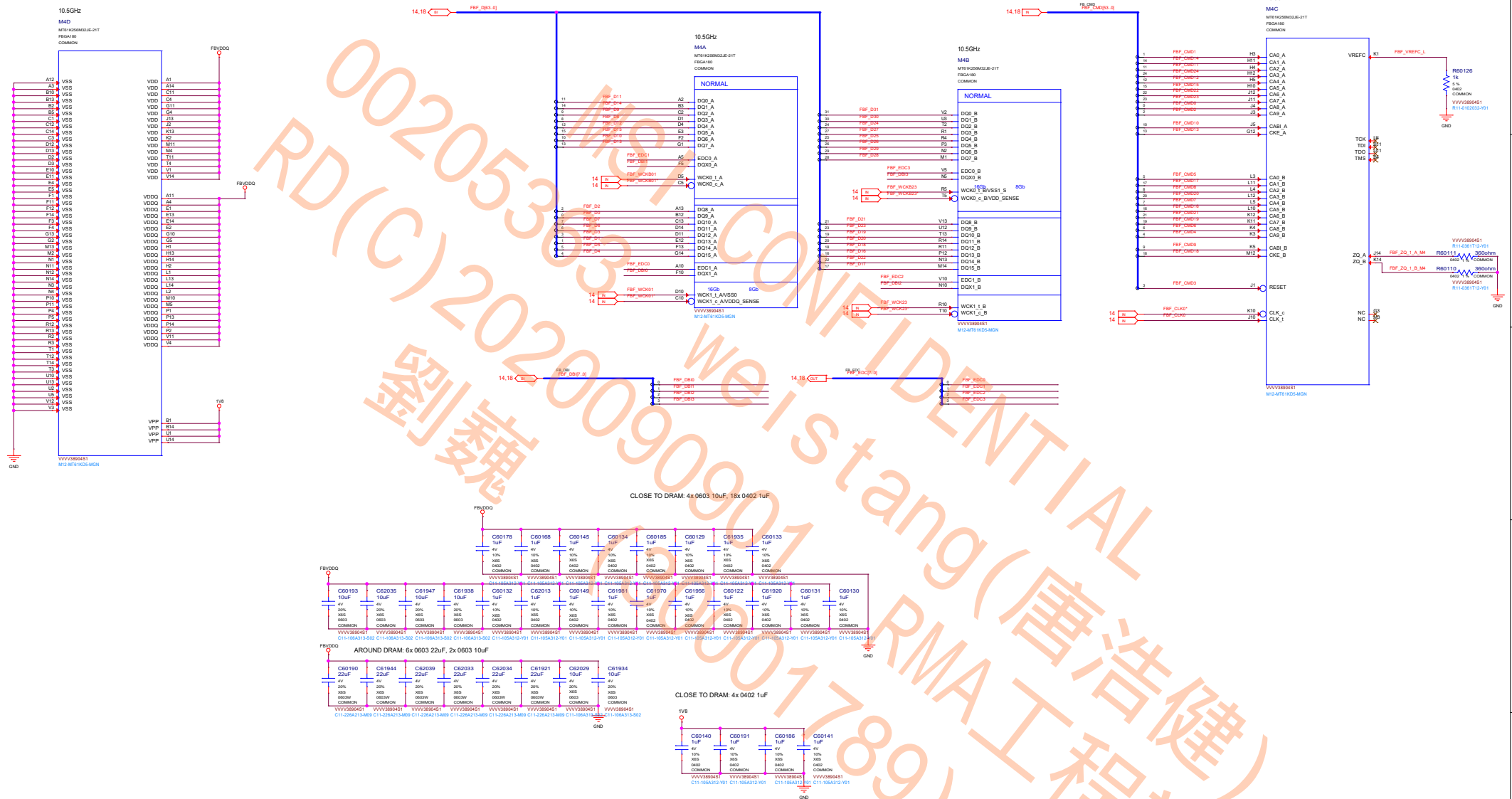
MEMORY: FBE Partition 31..0



MEMORY: FBE Partition 63..32



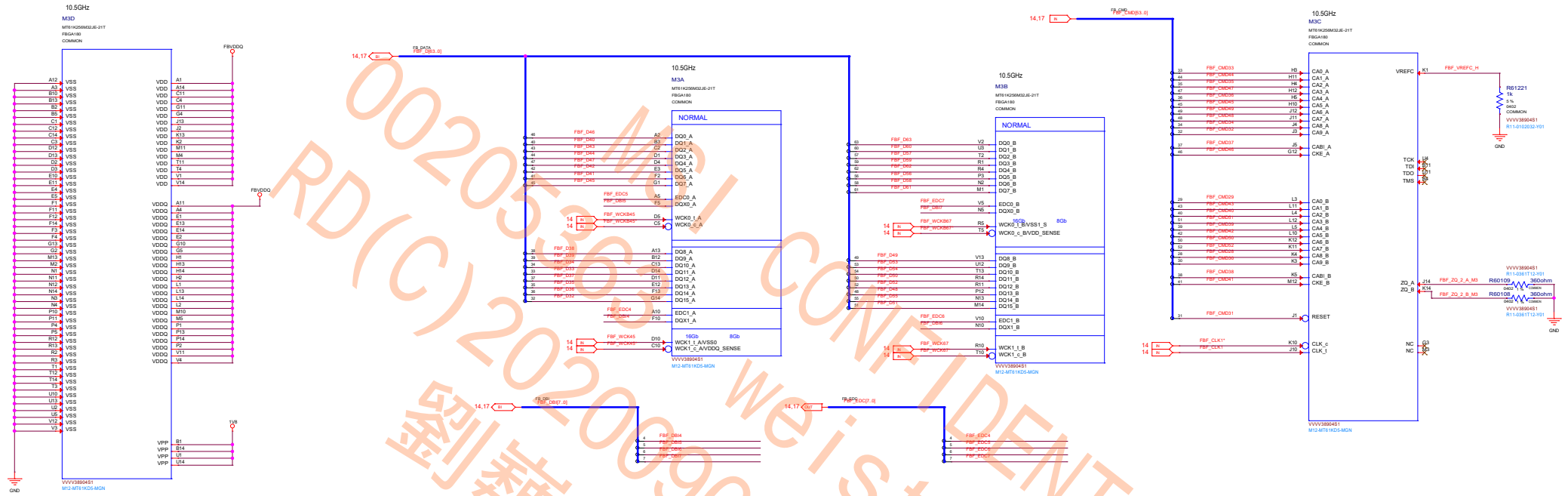
MEMORY: FBF Partition 31..0



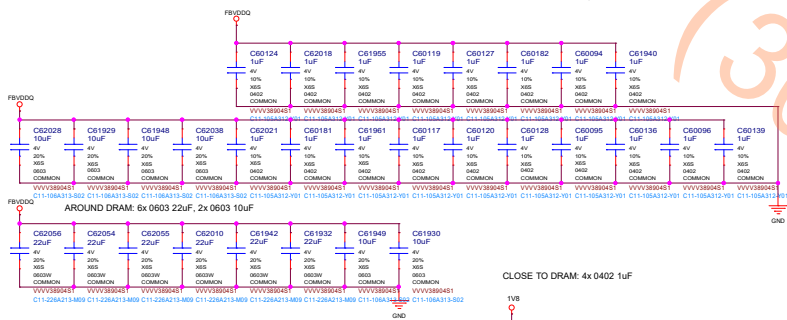
**MICRO-STAR INT'L CO.,LTD**

Size	Document Description	Rev
Custom	MEMORY: FBF Partition 31..0	2.1

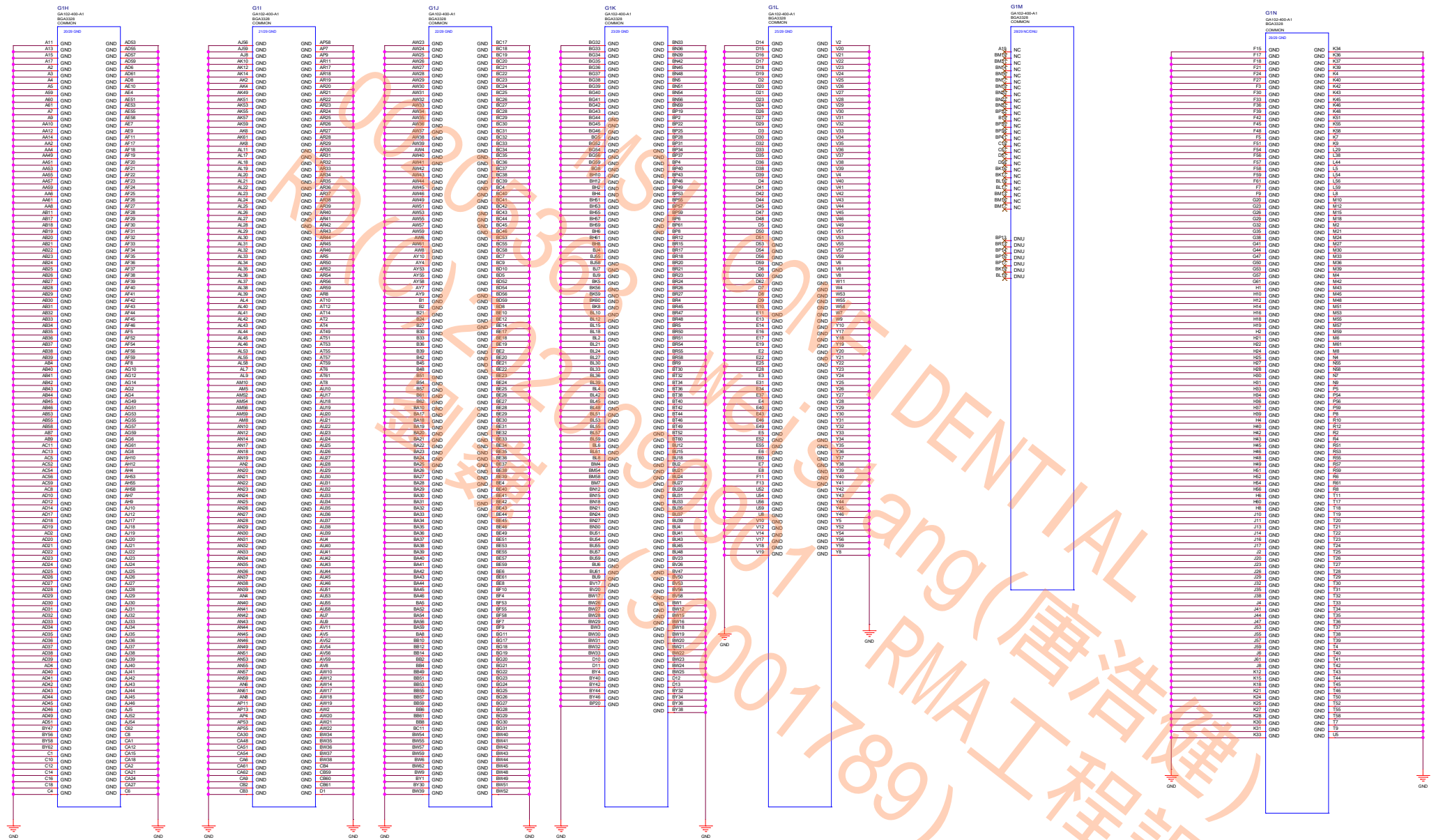
# MEMORY: FBF Partition 63..32



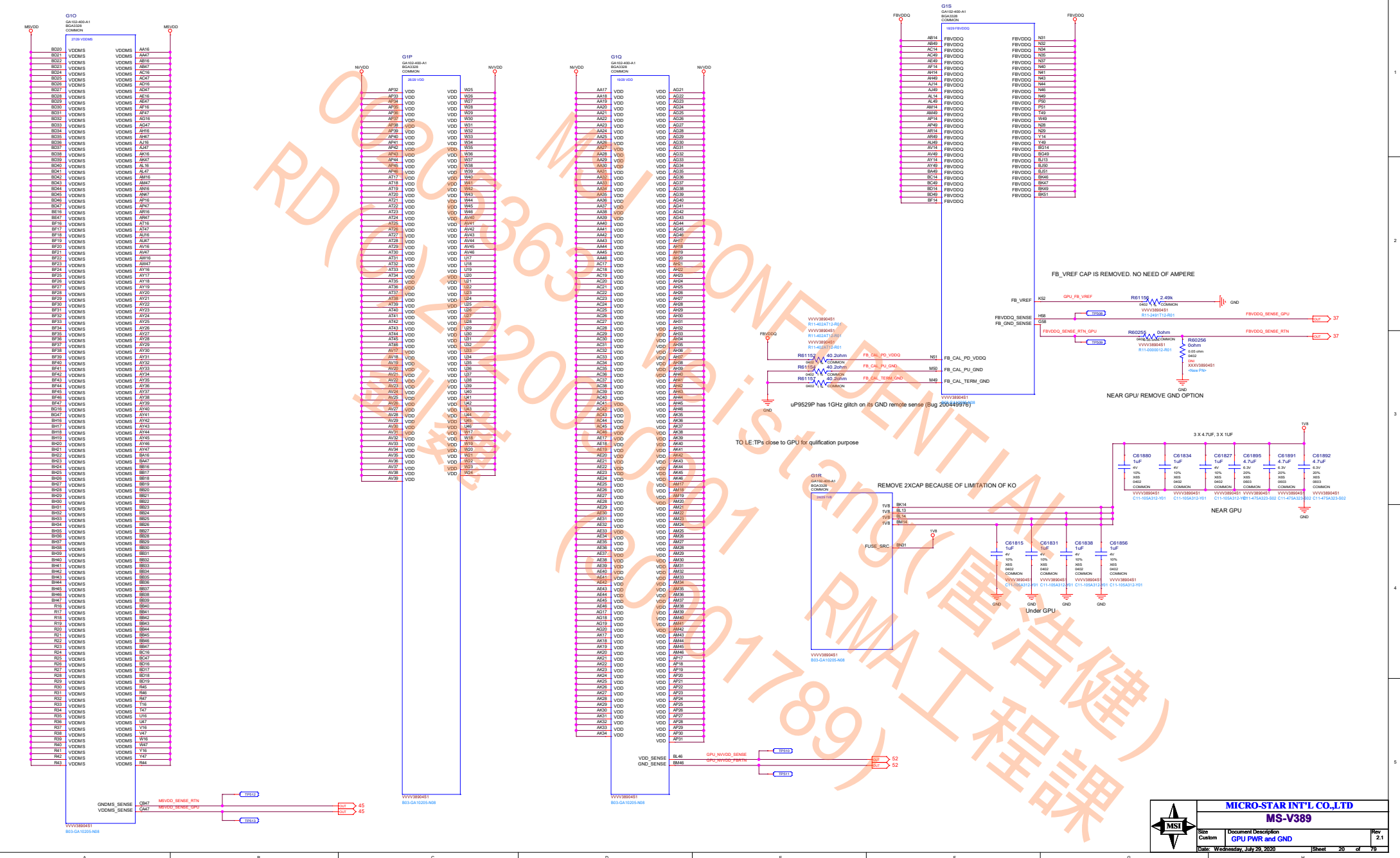
CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



## GPU GND, RFUs &amp; RSVD

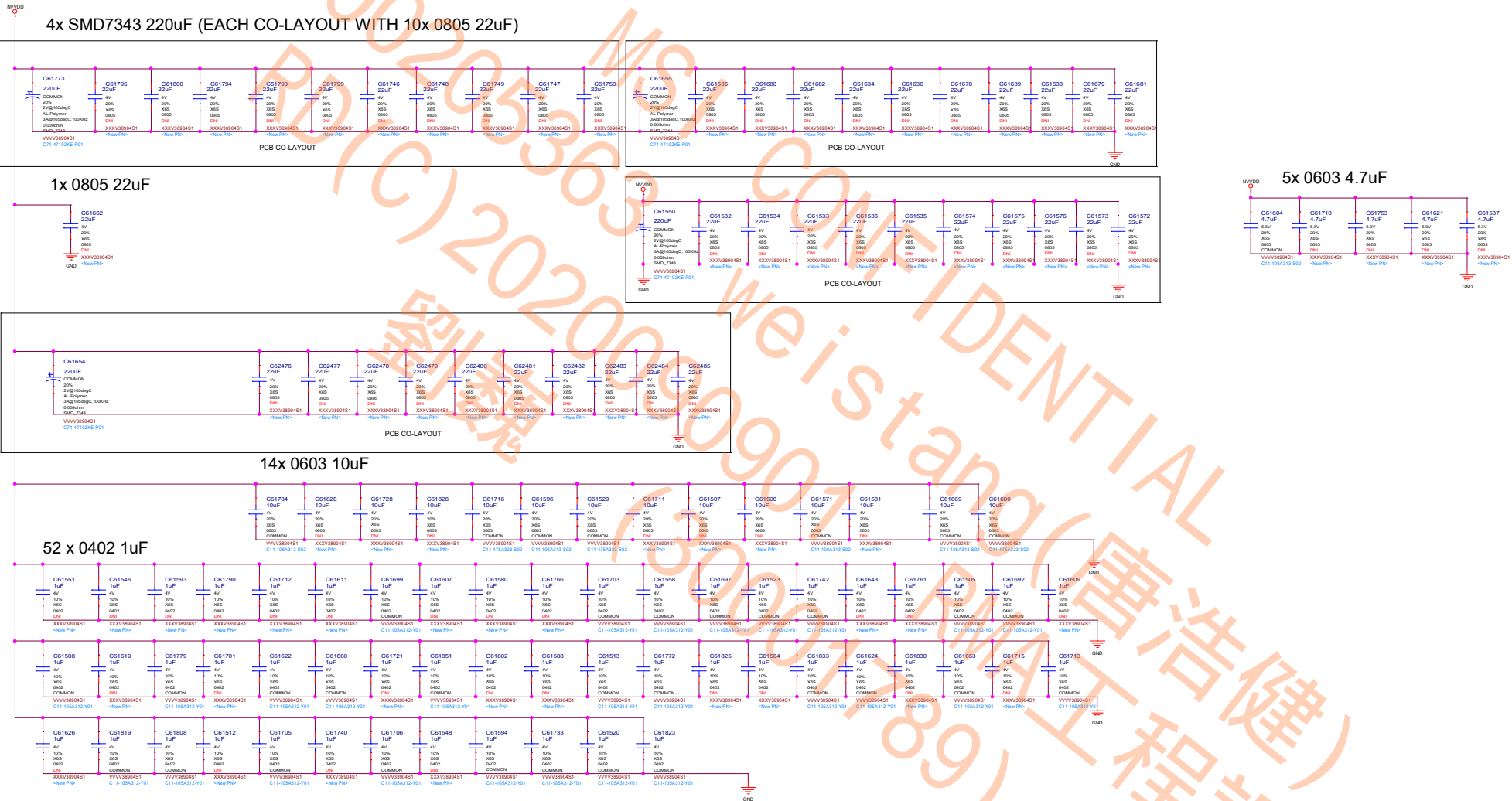


GPU PWR and GND

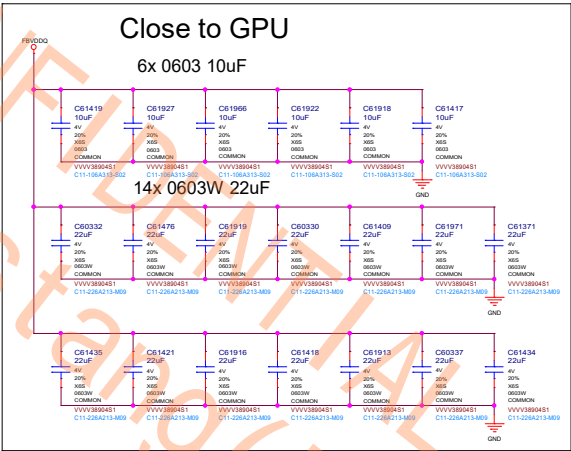
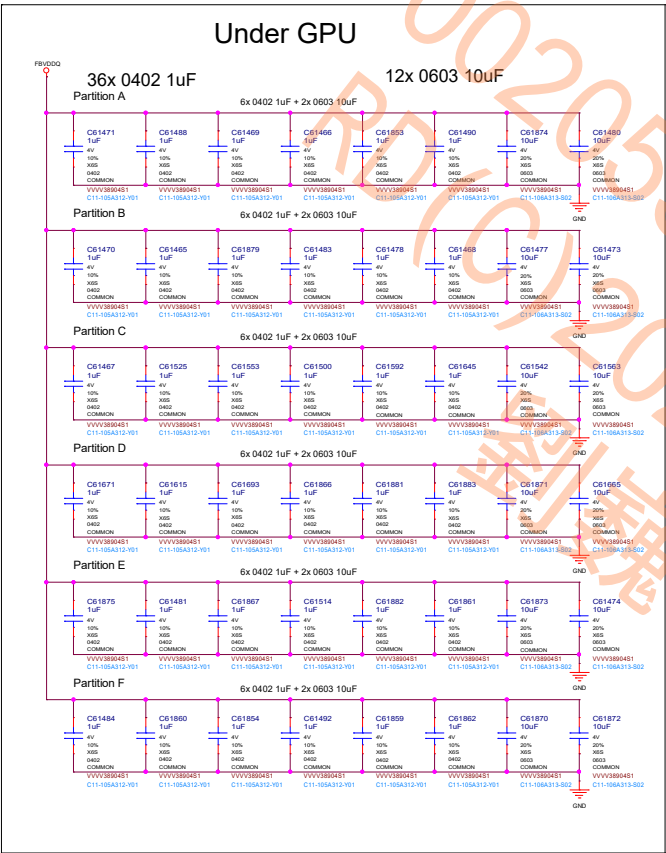




# NVVDD UNDER GPU

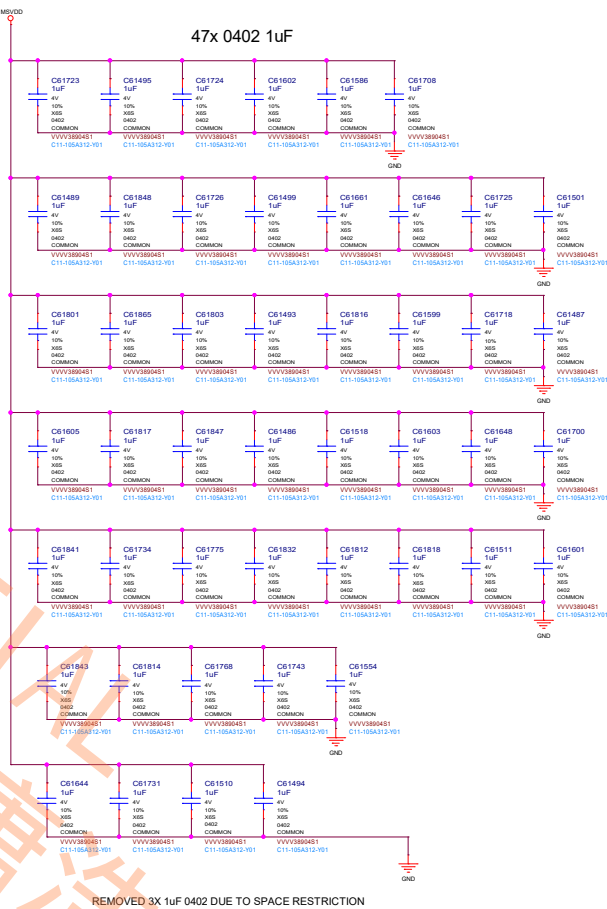
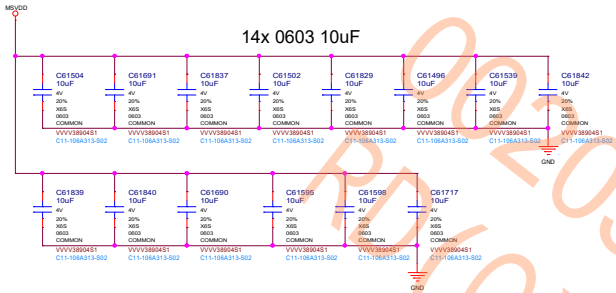


FBVDDQ

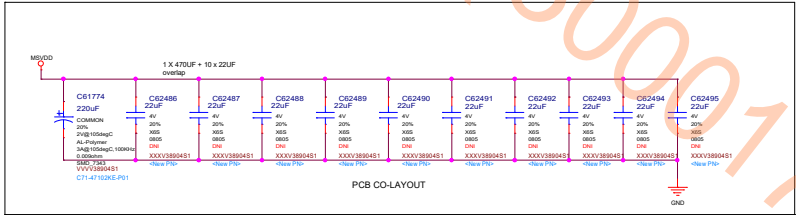
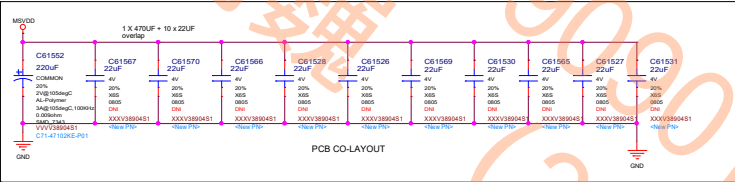


MSVDD

UNDER GPU



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



BLANK

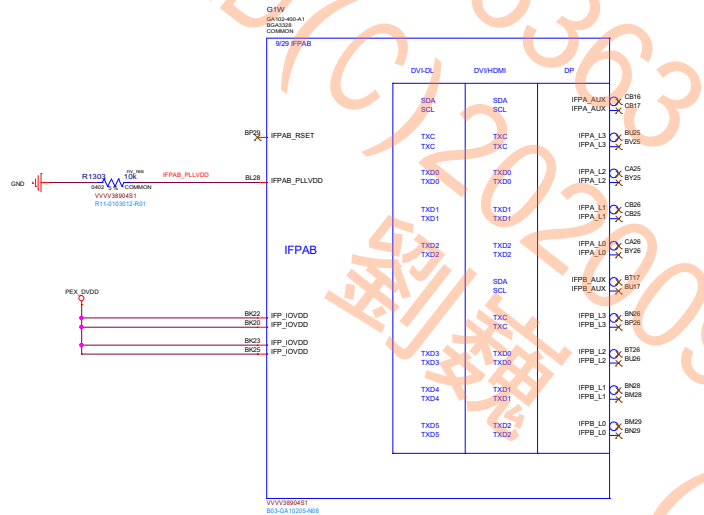
	MICRO-STAR INT'L CO.,LTD		
	MS-V389		
	Size	Document Description	Rev
	Custom	BLANK	2.1
Date: Wednesday, July 26, 2020		Sheet 24 of 79	

# NVHS Interface and FRAME LOCK





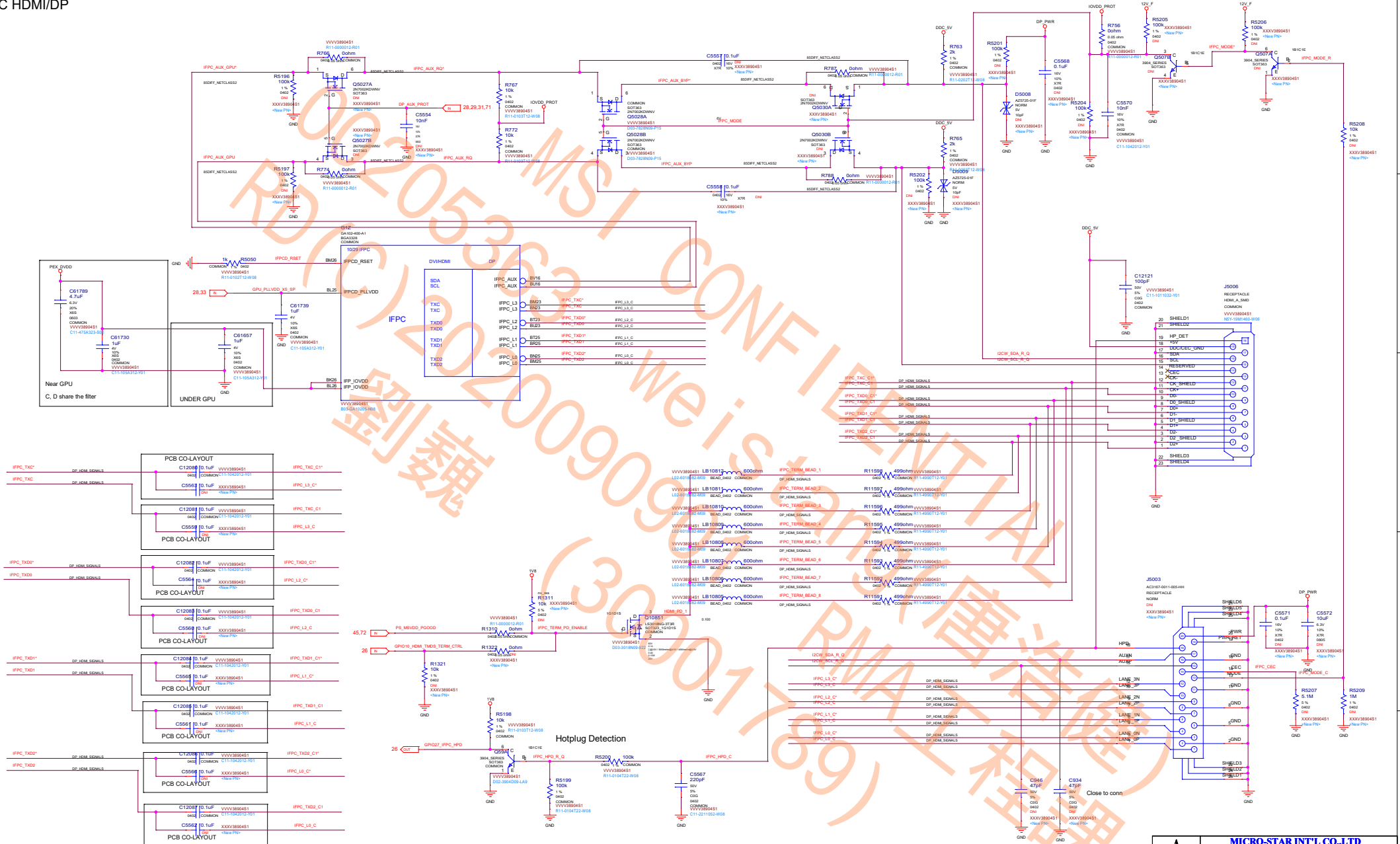








## IFPC HDMI/DP



**MICRO-STAR INT'L CO.,LTD**

MS-V389

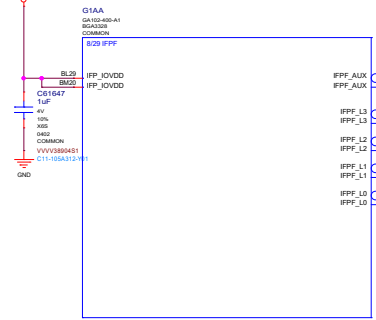
Size	Document Description	Rev
------	----------------------	-----

Custom	IFPC HDMI/DP	2.1
--------	--------------	-----

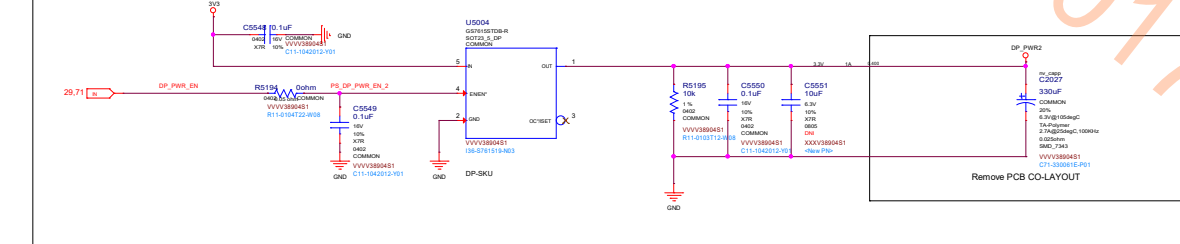
Date: Wednesday, July 29, 2020	Sheet 30 of 79
--------------------------------	----------------

# IFPF DP

## #41 SYMBOL BM20 to IFP\_IQVDD



## Fused DP\_PWR



Remove PCB CO-LAYOUT

MICRO-STAR INT'L CO.,LTD		
MS-V389		
Size	Document Description	Rev
Custom	IFPF DP	2.1
Date: Wednesday, July 26, 2020	Sheet	31 of 79

MISC: ROM, Straps

GROUP0 STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
H	L	L	00100	RAMCFG MICRON 8Gb G6X 19Gbps x8 (161-0430-900)
H	L	H	00101	RAMCFG MICRON 8Gb G6X 21Gbps x8 (161-0431-900)
L	L	M	01000	RAMCFG MICRON 8Gb G6X 20Gbps x16 (161-0424-900)
L	L	H	00001	RAMCFG MICRON 8Gb G6X 21Gbps x16 (161-0431-900)
L	M	H	01010	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0]_FS_OVERT	1.ENABLE 0.DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

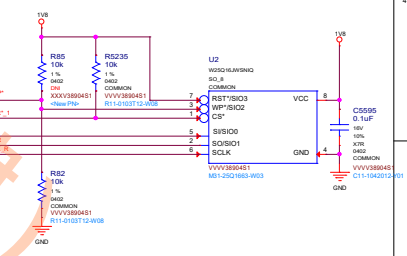
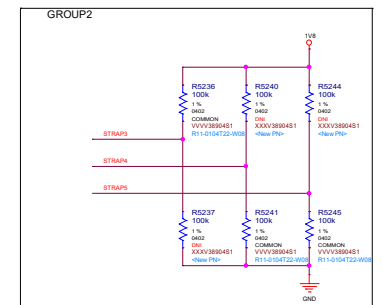
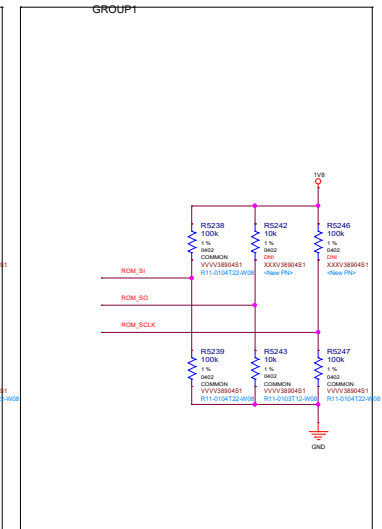
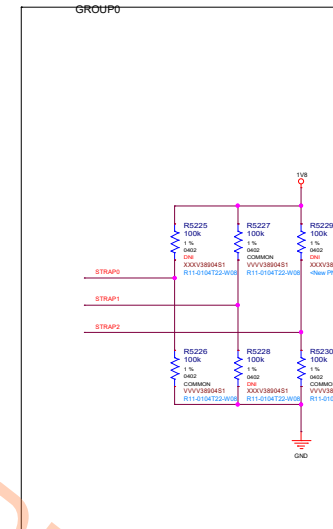
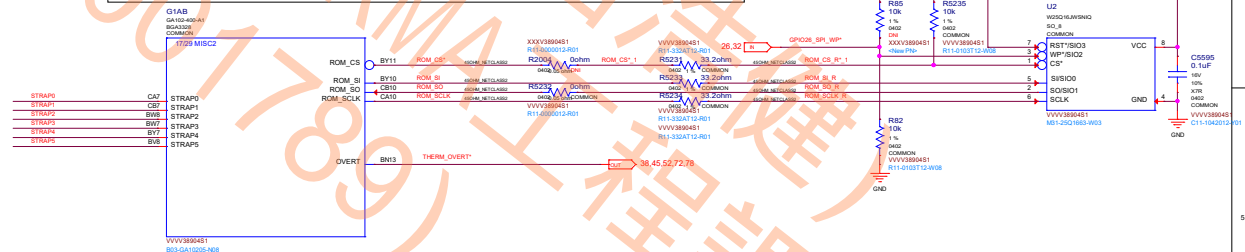
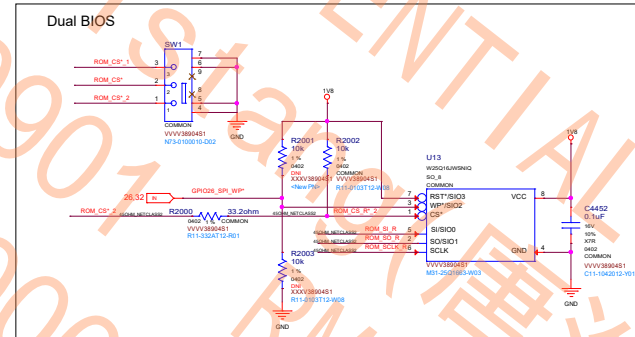
DEFAULT

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE

1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGNAL

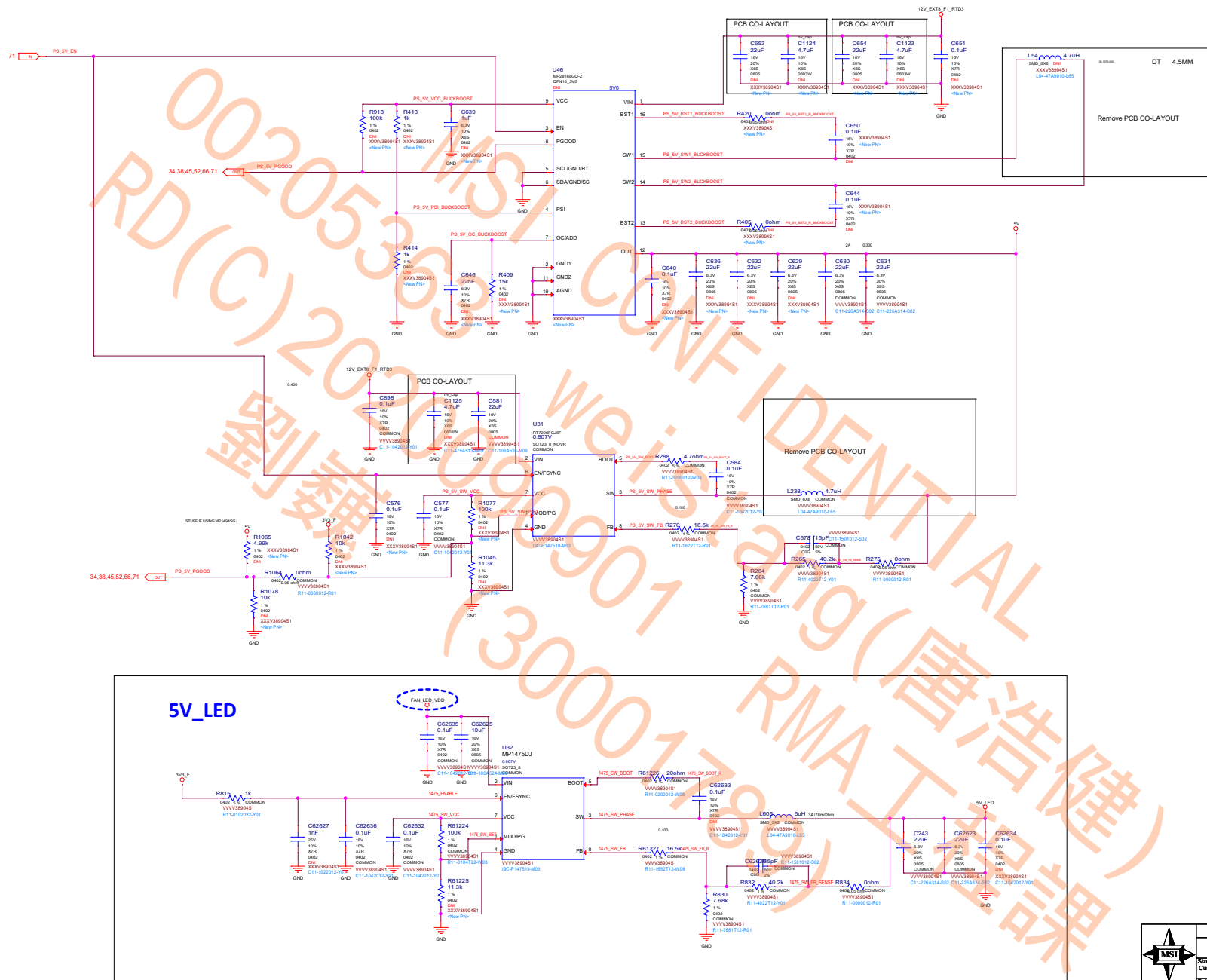
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER

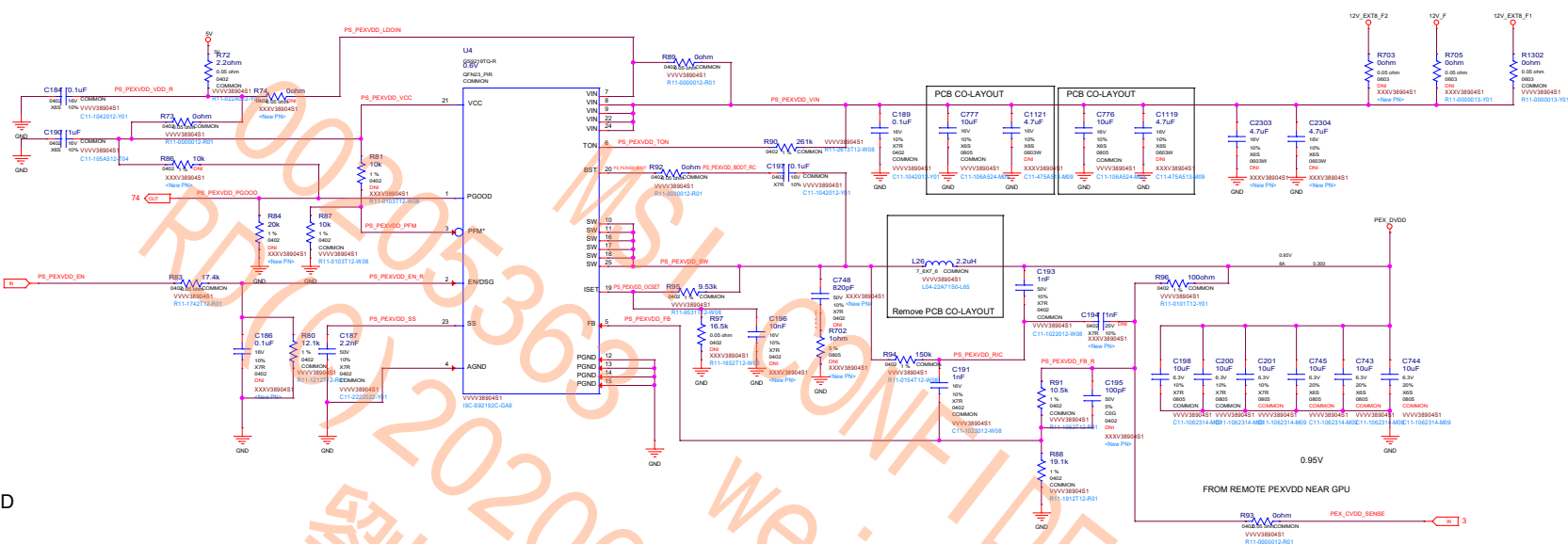
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



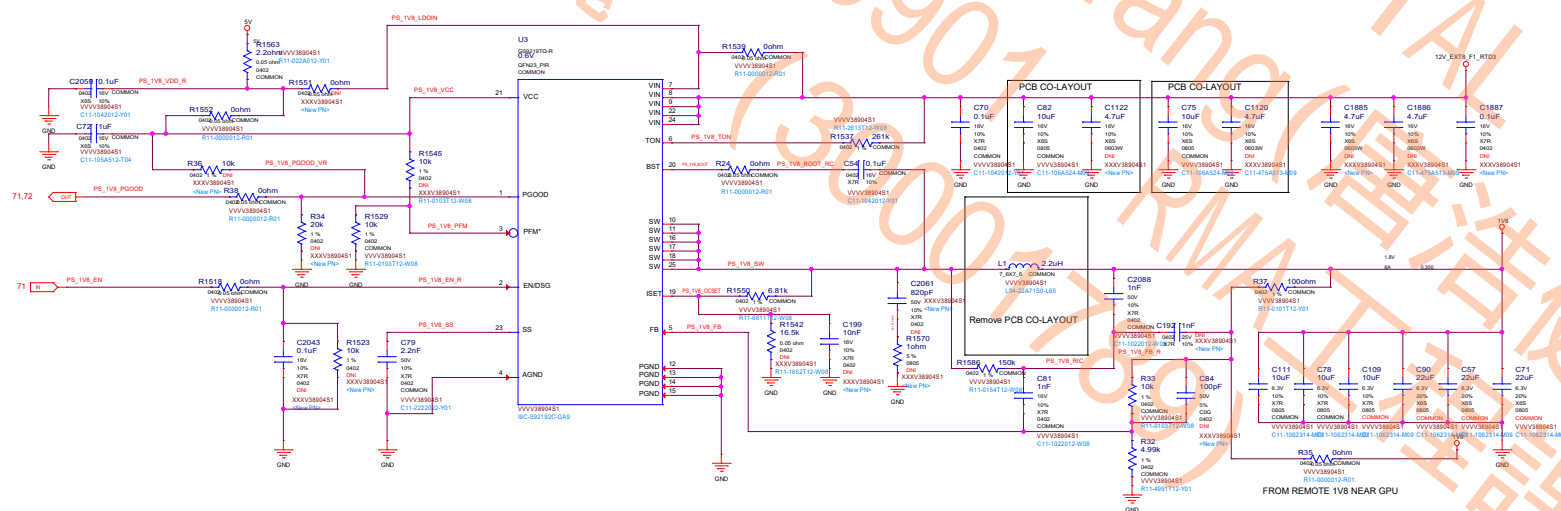









PEX DVDD



1V8

BLANK

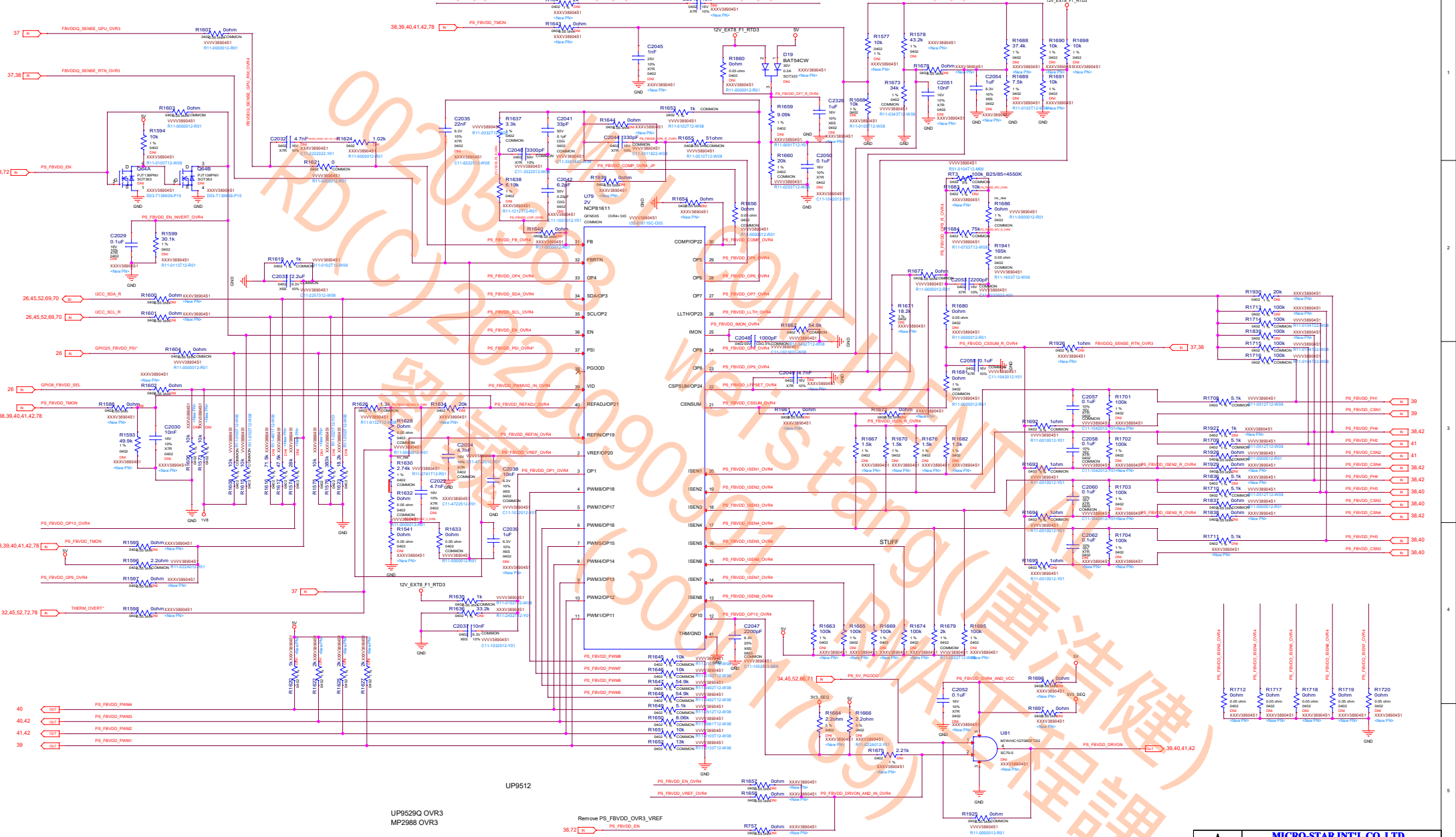
MSI CONFIDENTIAL  
00205363  
RD(C) 2020090901  
唐浩健  
(30001789)  
RMA工程課

	MICRO-STAR INT'L CO.,LTD		
	MS-V389		
	Size	Document Description	Rev
	Custom	BLANK	2.1
Date: Wednesday, July 29, 2020		Sheet	38 of 79

### Remove FBVDD Controller OVR3



## PS:FBVDDQ OVR4



UP9529Q OVR:  
MP2988 OVR3

Remove PS\_FBVDD\_OVR3\_VRE



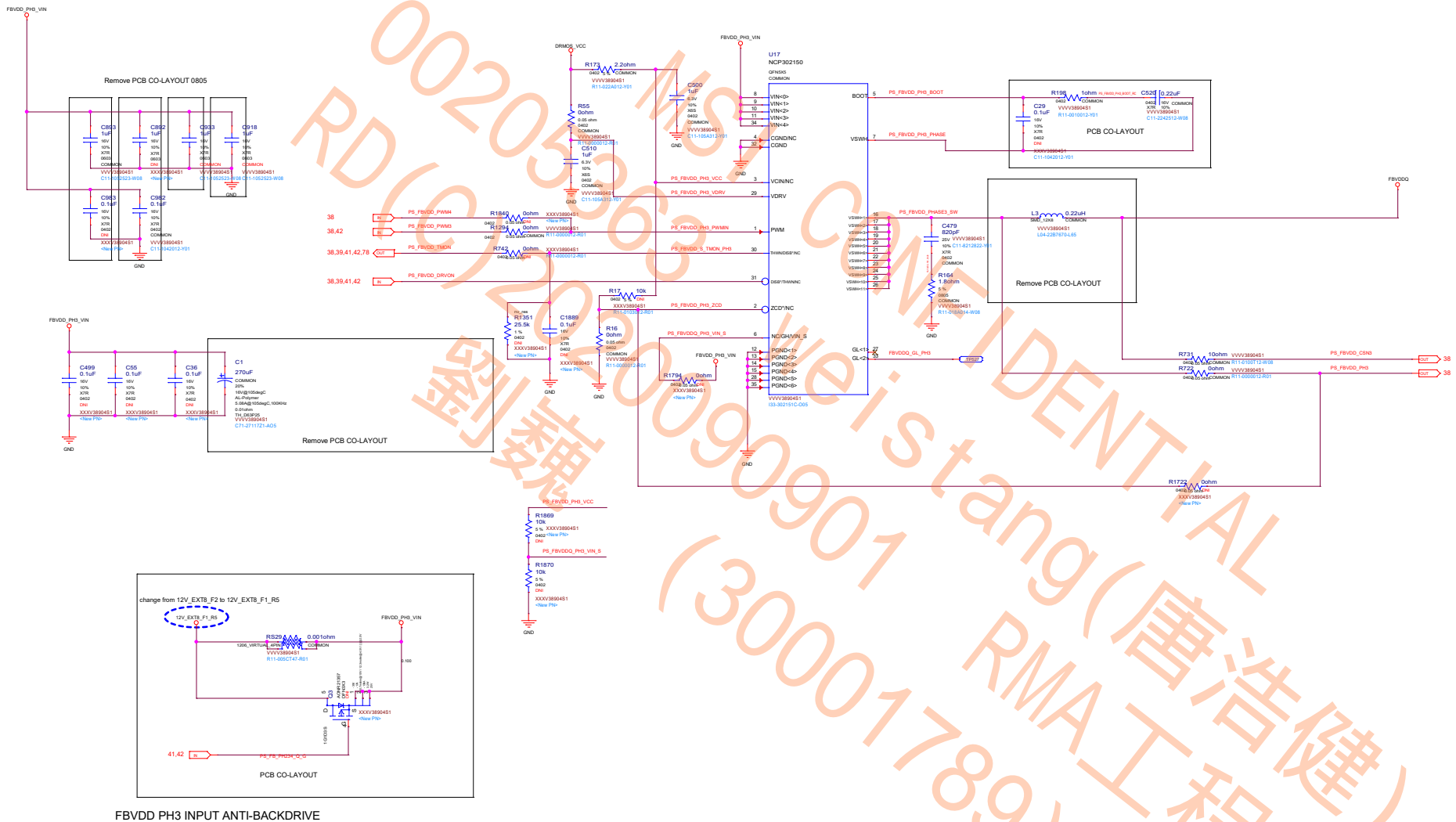
**MICRO-STAR INT'L CO.,LTD**  
**MS-V389**

Size Custom	Document Description <b>PS:FBVDDQ OVR4</b>	Rev 2.1
Date: Wednesday, July 29, 2020		Sheet 38 of 79



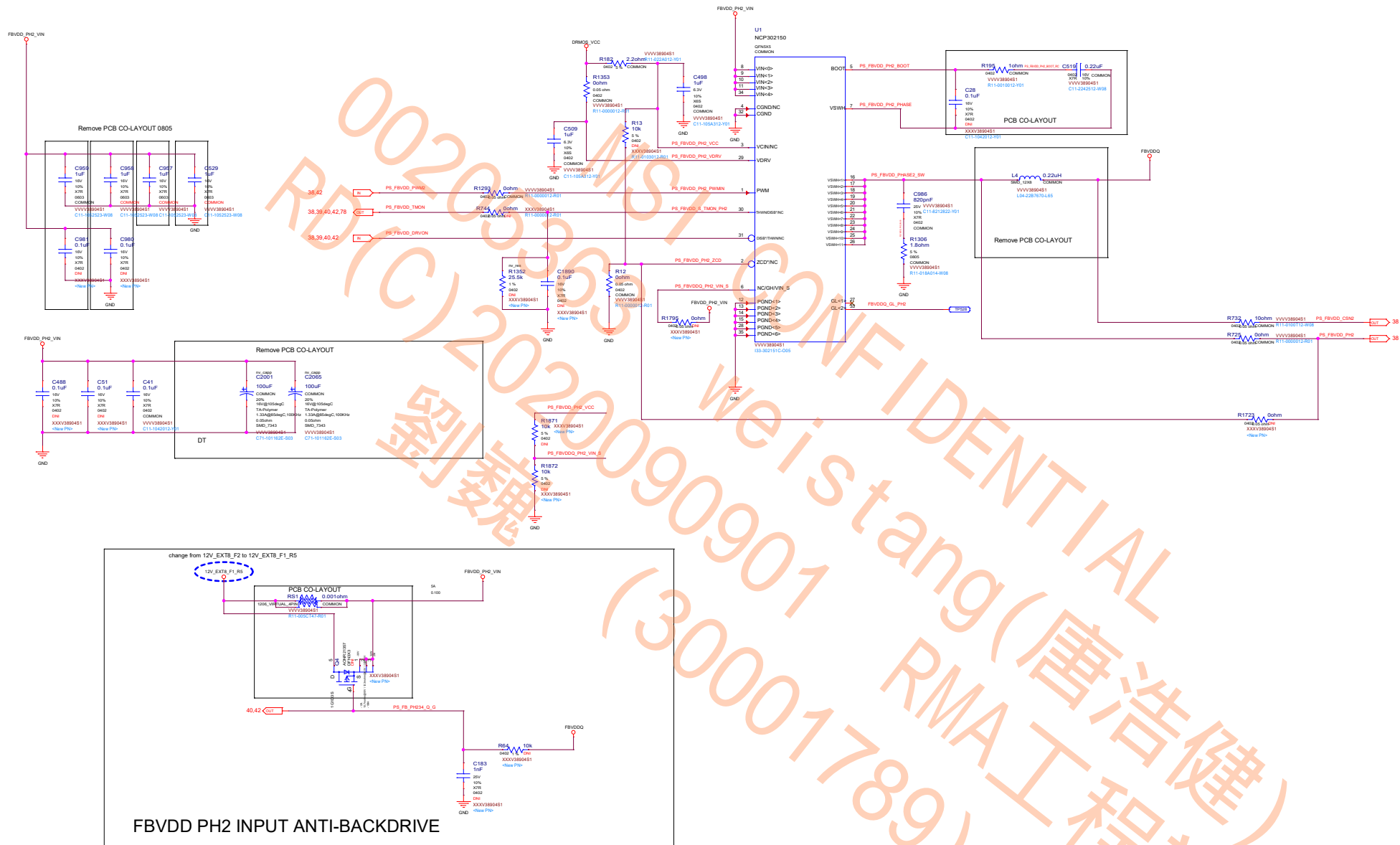


## PS: FBVDD PH3



### FBVDD PH3 INPUT ANTI-BACKDRIVE

## PS: FBVDD PH2



**MICRO-STAR INT'L CO.,LTD**

MS-V389

Size	Document Description	Rev
------	----------------------	-----

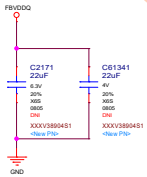
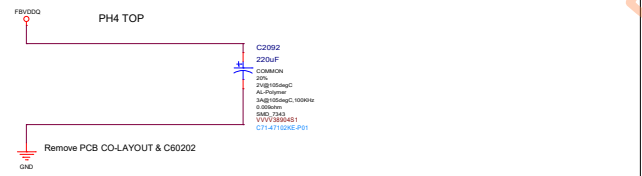
Custom	PS: FBVDD PH2	2.1
--------	---------------	-----

Date: Wednesday, July 29, 2020	Sheet 41 of 79
H	

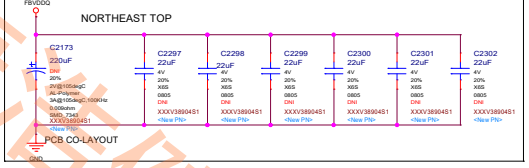
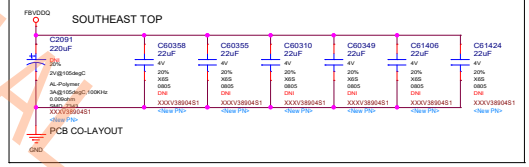
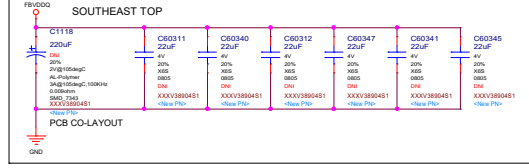
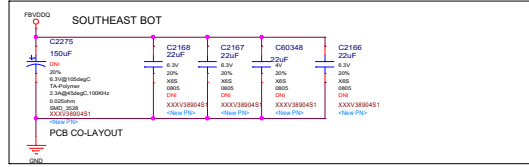
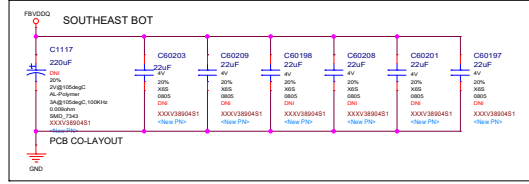
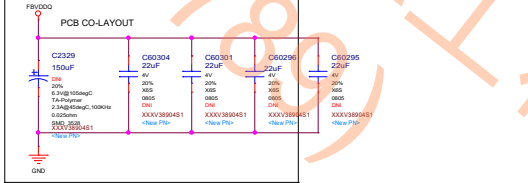
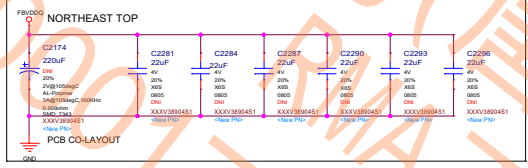
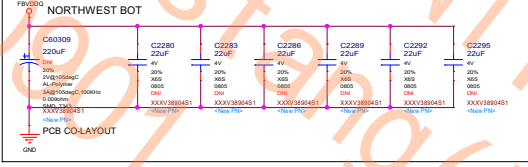
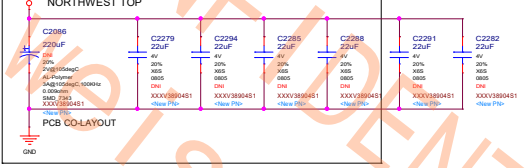
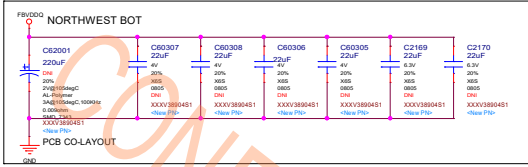
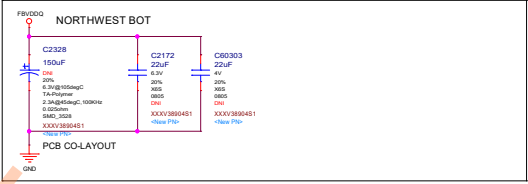


PS: FBVDD OUTPUT CAP

3x 820uF TH FBVDD OUTPUT BULK CAPS

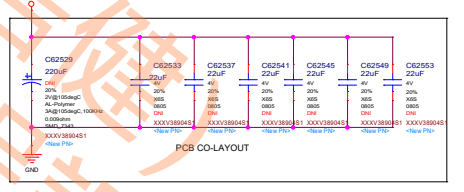
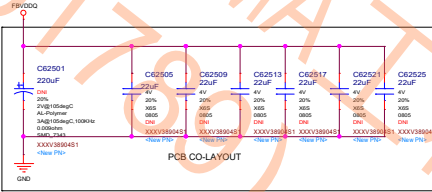
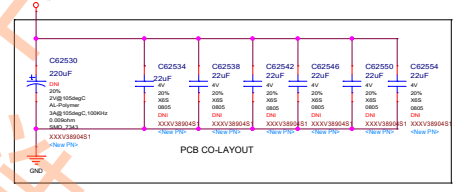
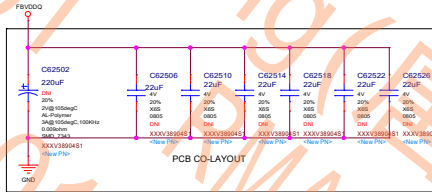
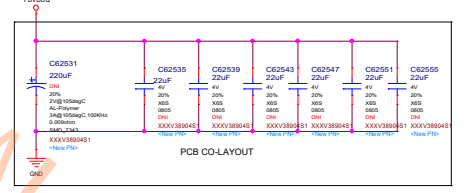
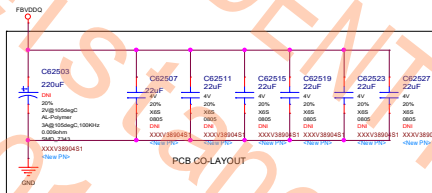
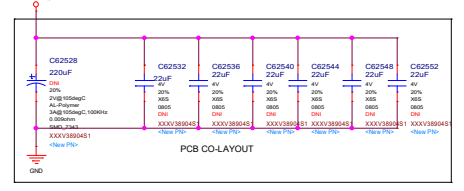
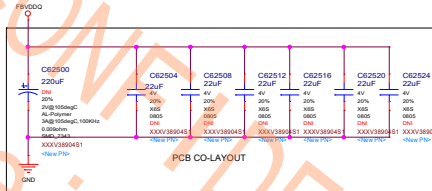
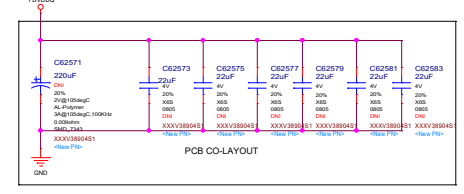
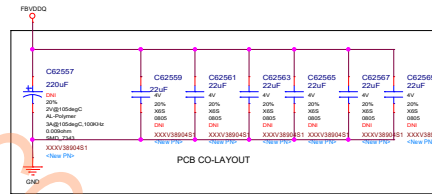
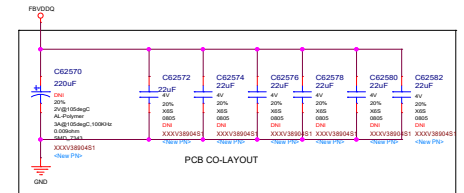
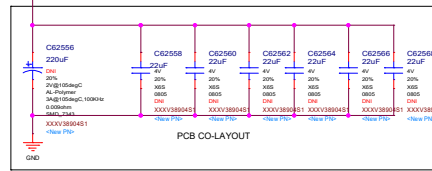


CLOSE TO FB PH3 OUTPUT STUFF



## Added for A01 x16

ADDED FOR A00 X16 DESIGN: PLACE UNDER MEMORIES



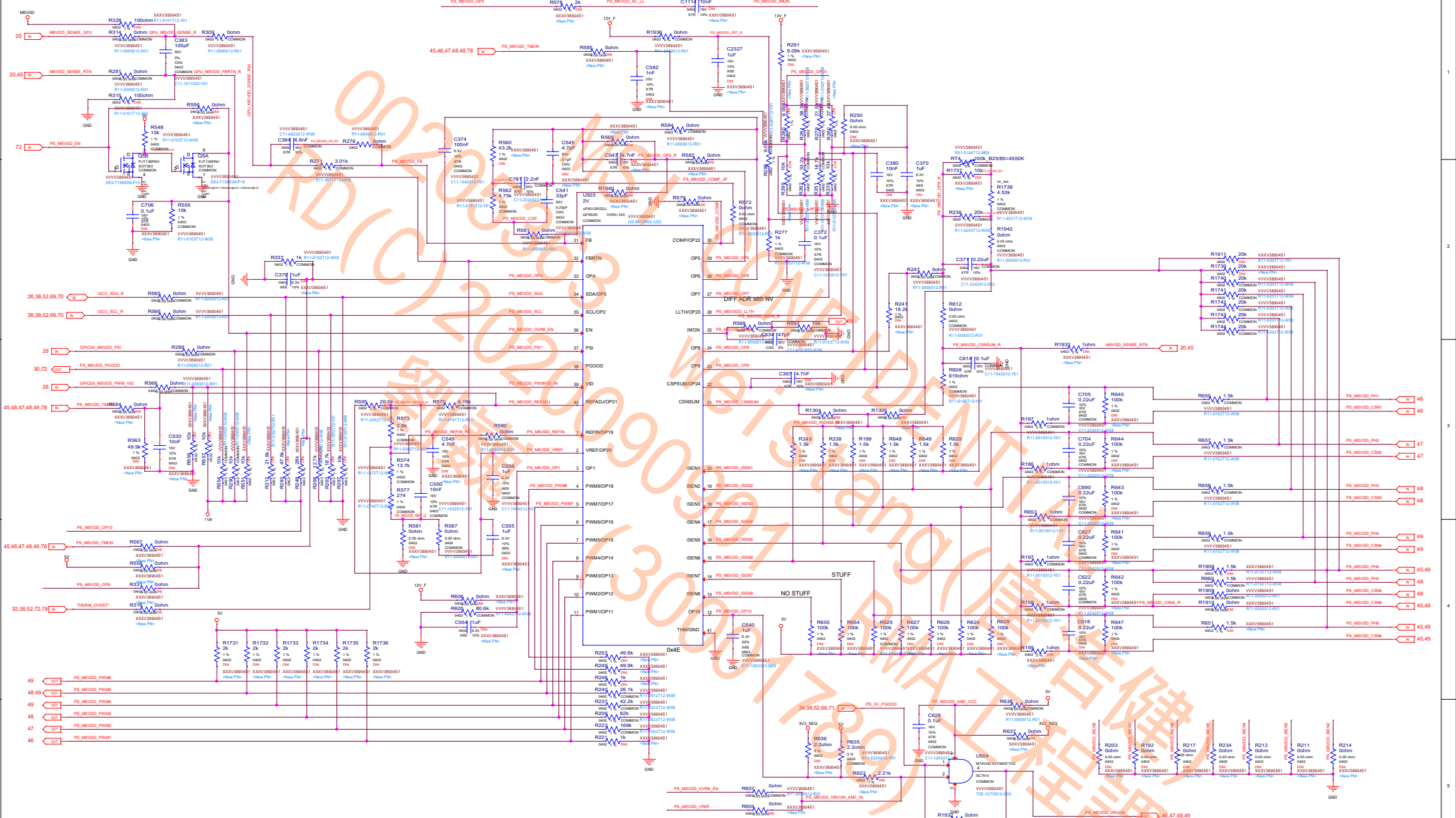
MICRO-STAR INT'L CO., LTD

MS-V389

Rev	Doc Description	Rev
Custom	PS_FBVDD_OUTPUT_CAP_NEAR_MEM	2.1

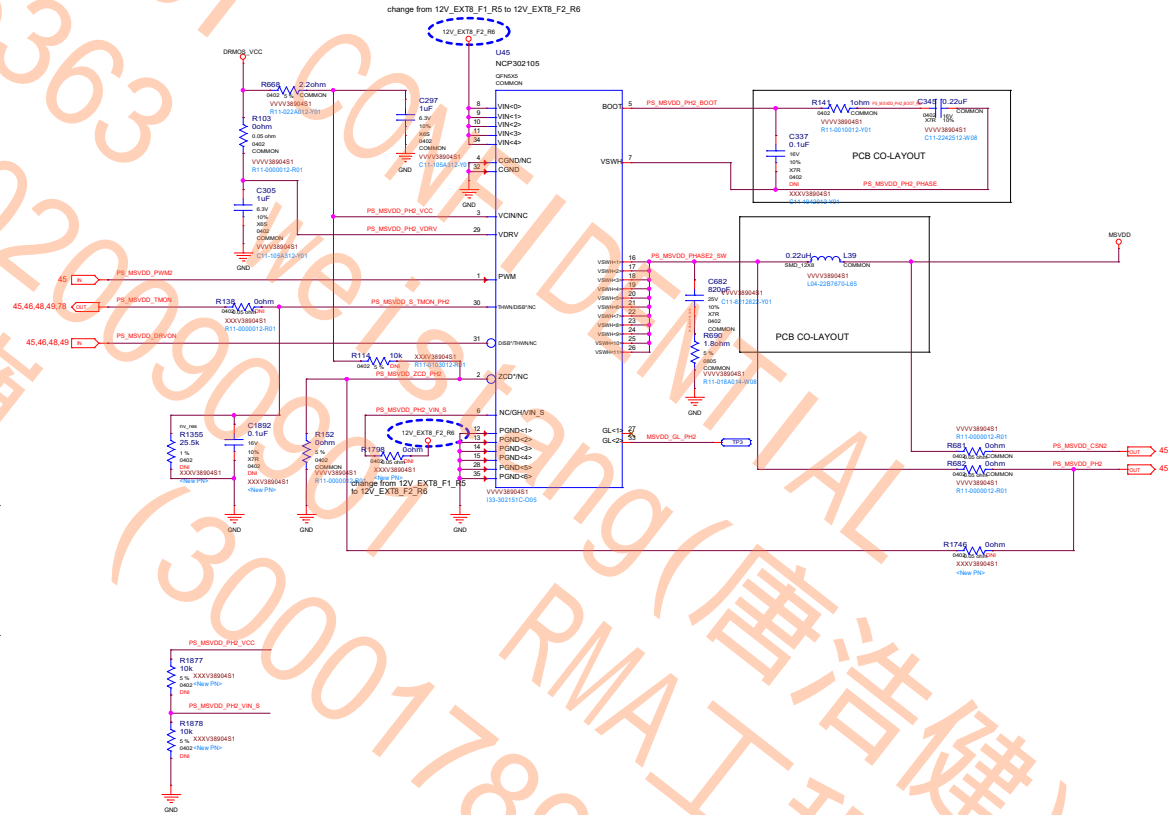
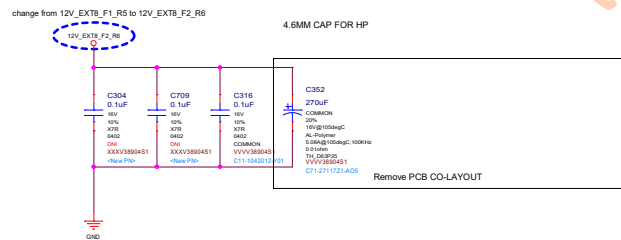
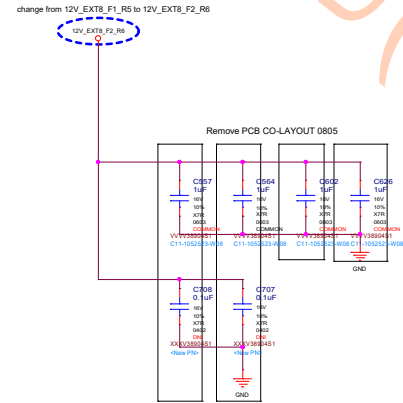
Date: Wednesday, July 25, 2020 Sheet 44 of 76

## PS: MSVDD







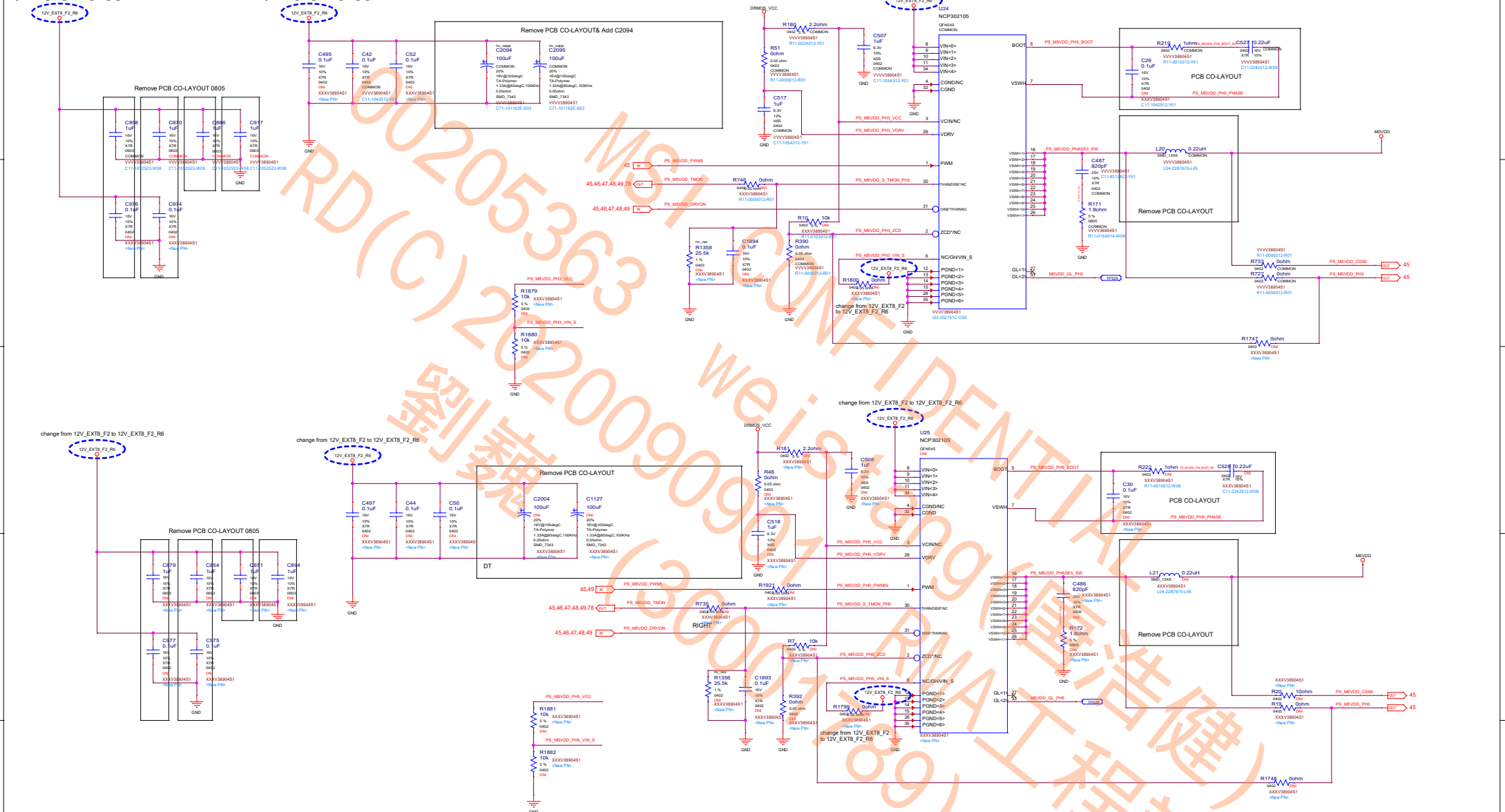


# PS:MSVDD Phase 3, 5

change from 12V\_EXT8\_F2 to 12V\_EXT8\_F2\_R6

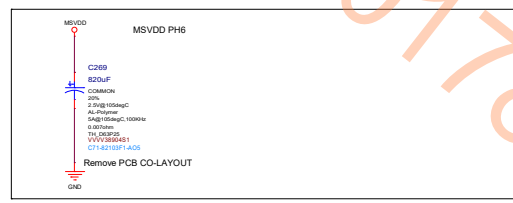
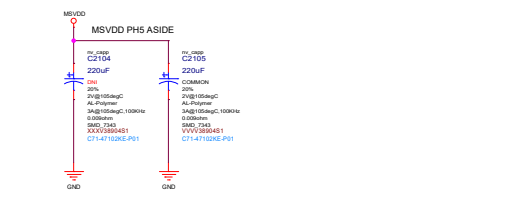
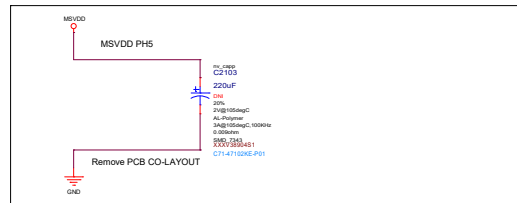
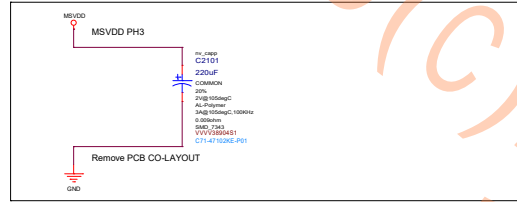
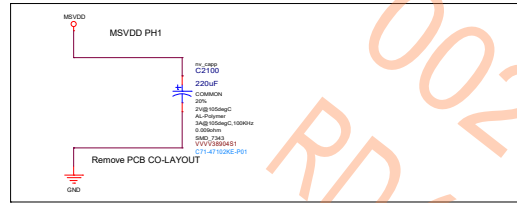
change from 12V\_EXT8\_F2 to 12V\_EXT8\_F2\_R6

change from 12V\_EXT8\_F2 to 12V\_EXT8\_F2\_R6






PS:MSVDD OUTPUT CAP (TOP)

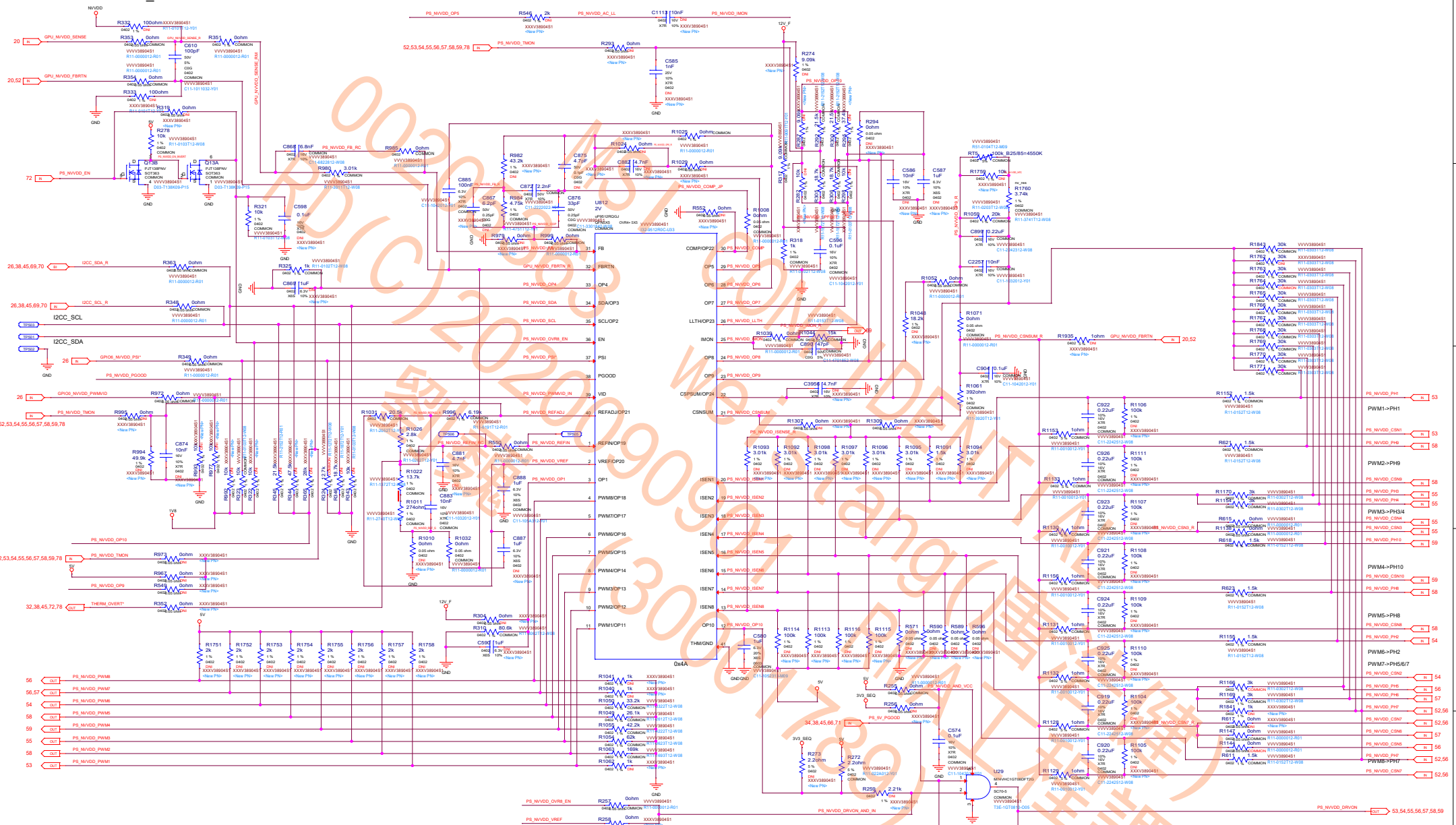


BLANK

MSI CONFIDENTIAL  
00205363  
RD(C) 2020090901  
Weistang (唐浩健)  
(30001789)  
RMA工程課

	MICRO-STAR INT'L CO.,LTD		
	MS-V389		
	Size	Document Description	Rev
	Custom	BLANK	2.1
Date: Wednesday, July 26, 2020		Sheet	51 of 79

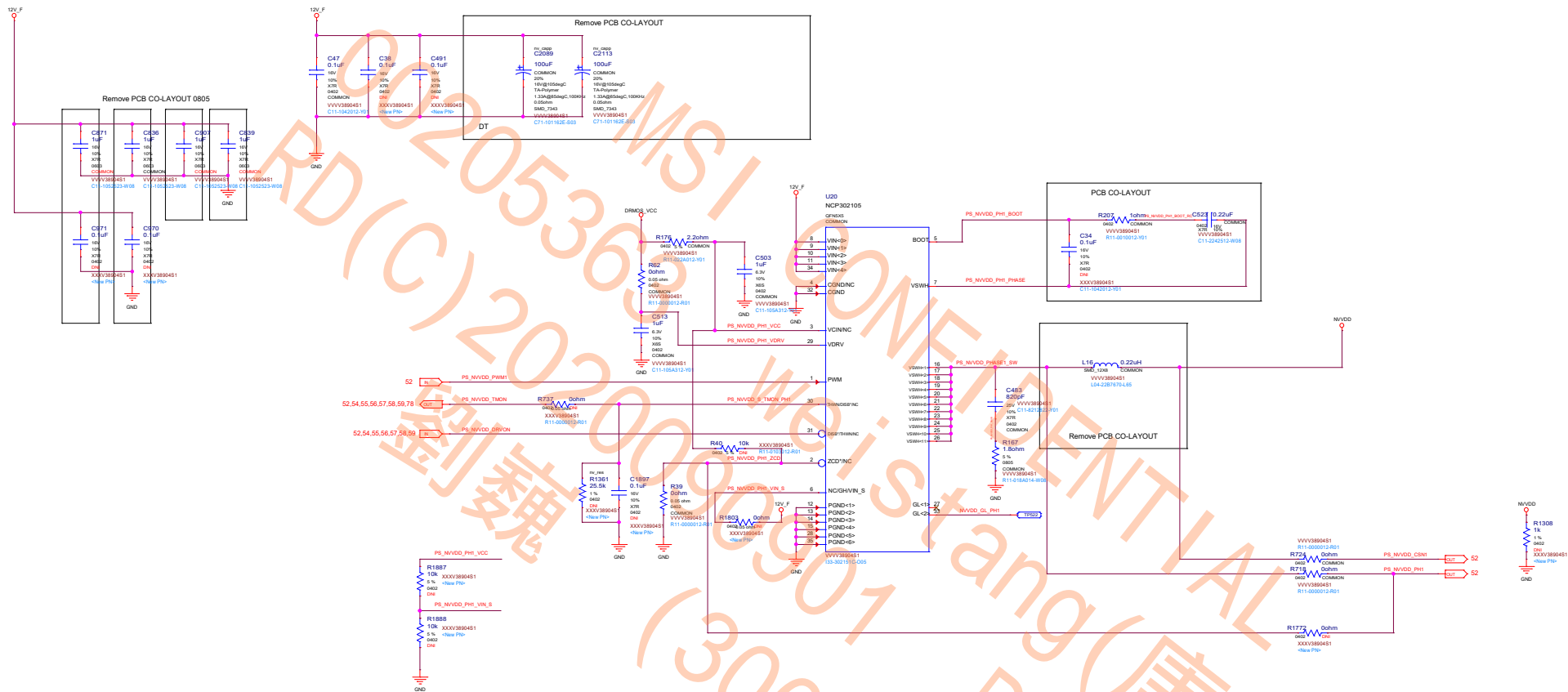
## PS: NVVDD Controller\_OVR8



**MICRO-STAR INT'L CO.,LTD**

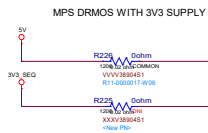
MS-V389

Size	Document Description	Rev
Custom	PS: NVDD Controller_OVR8	2.1

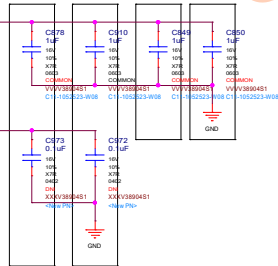




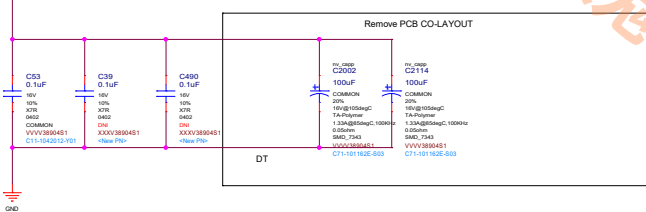
## PS: NVVDD Phase 2



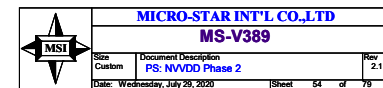
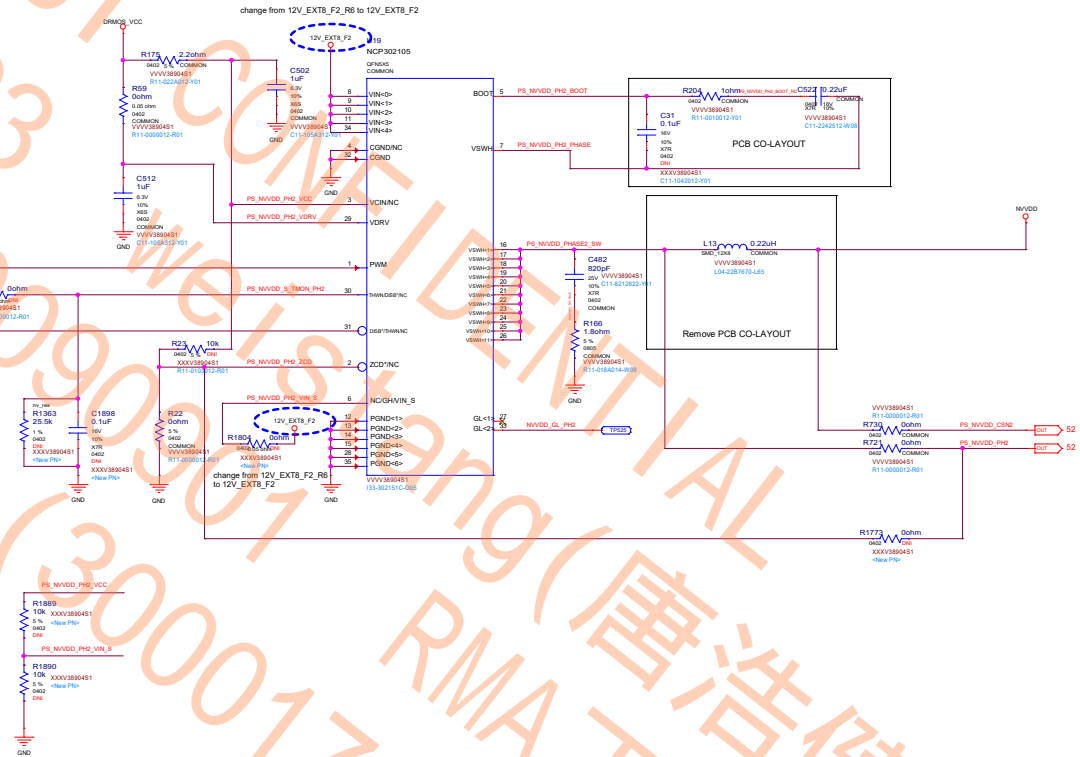
change from 12V\_EXT8\_F2\_R6 to 12V\_EXT8\_F2



change from 12V\_EXT8\_F2\_R6 to 12V\_EXT8\_F2

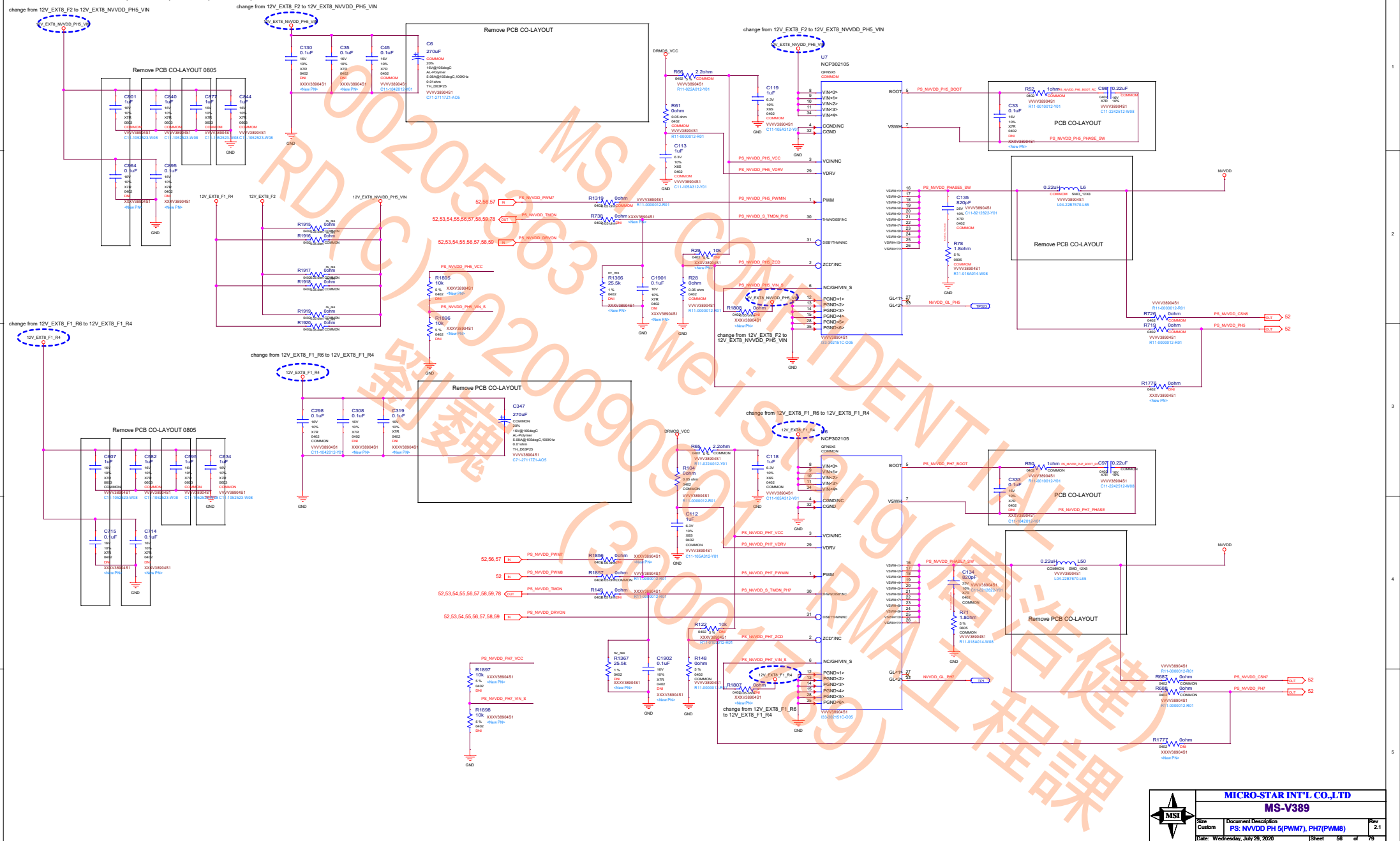


Remove 12V\_EXT8\_NVVDD\_PH2\_VIN option





PS: NVVDD PH 5(PWM7), PH7(PWM8)



**MICRO-STAR INT'L CO.,LTD**  
**MS-V389**

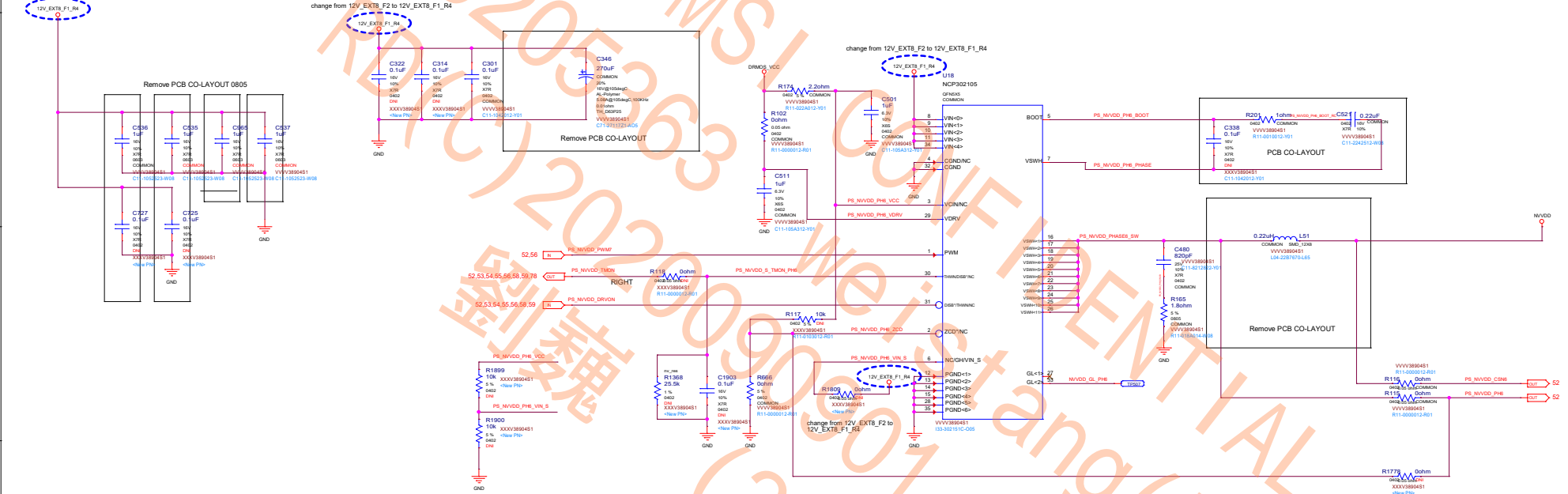
Size Custom	Document Description <b>PS: NVDD PH 5(PWM7), PH7(PWM8)</b>	Rev 2.1
Date: Wednesday, July 29, 2020	Sheet 56 of 79	

# PS: NVVDD Phase 6(PWM7)

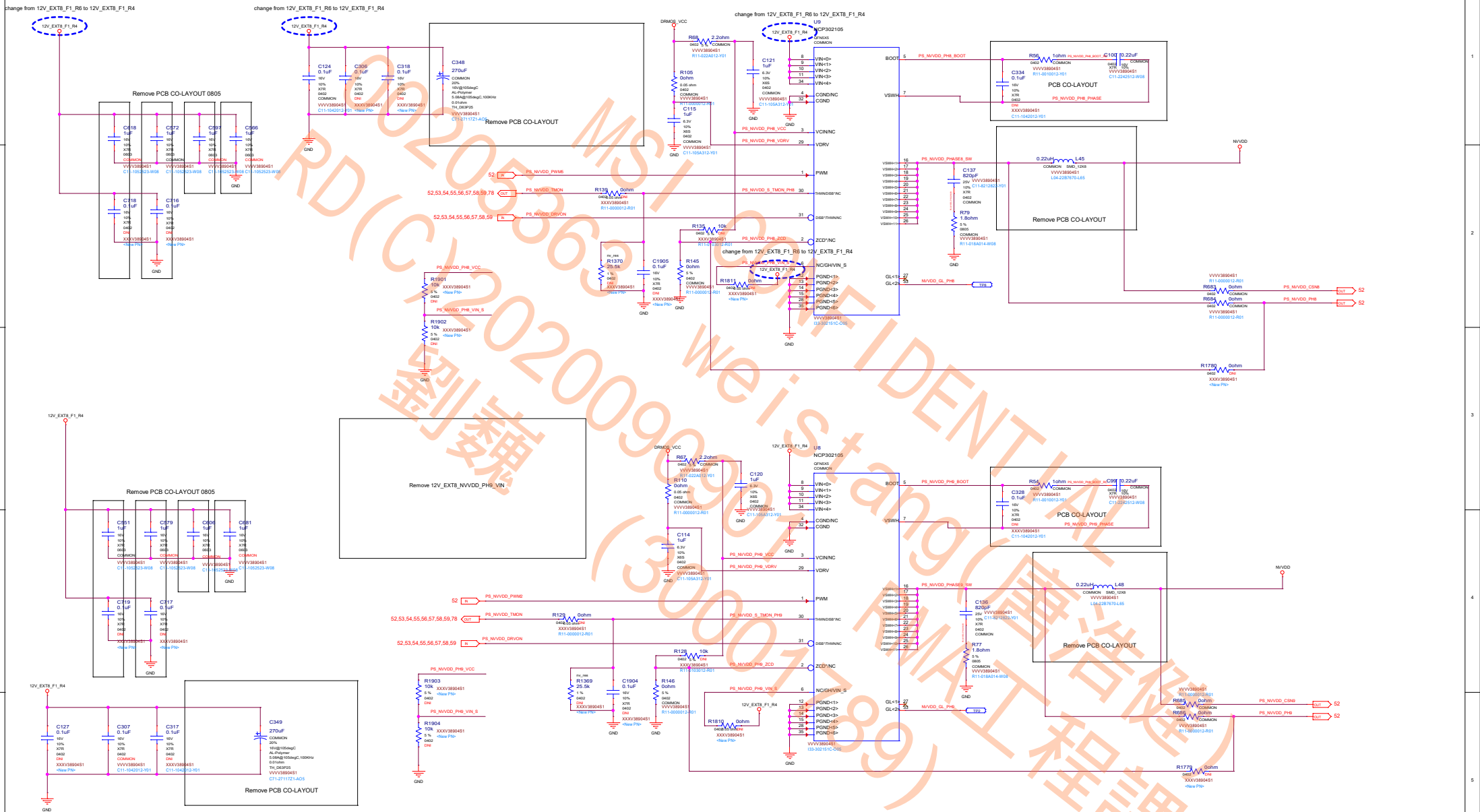
change from 12V\_EXT8\_F2 to 12V\_EXT8\_F1\_R4

change from 12V\_EXT8\_F2 to 12V\_EXT8\_F1\_R4

change from 12V\_EXT8\_F2 to 12V\_EXT8\_F1\_R4

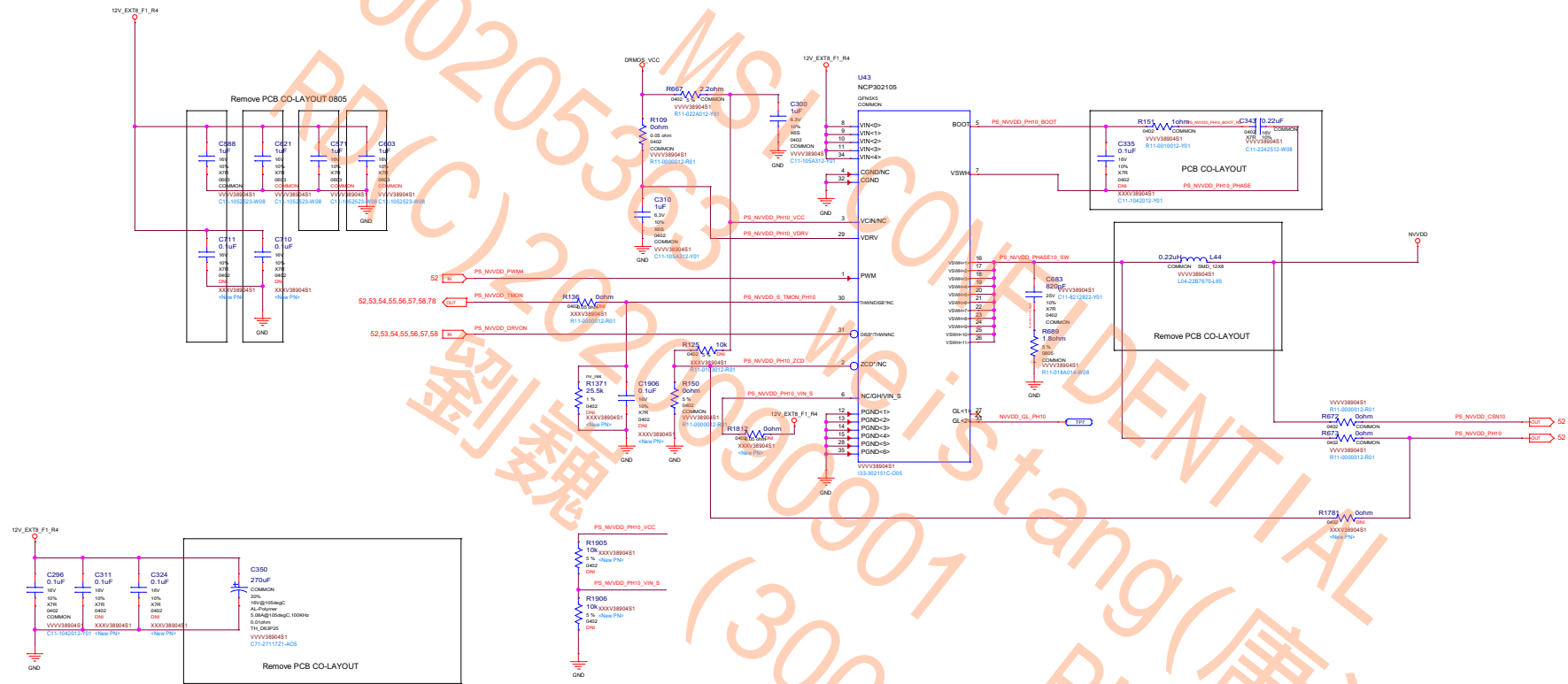


## PS: NVVDD PH 8 (PWM5), PH 9(PWM2)



**MICRO-STAR INT'L CO.,LTD**  
**MS-V389**

Size Custom	Document Description PS: NVDD PH 8 (PWM5), PH 9(PWM2)	Rev 2.1
Date: Wednesday, July 29, 2020	Sheet 58 of 79	



PCB CO-LAYOUT

C131, C132, C133, C140, C141, C142, C2106, C2107, C2133, C2134, C2135, C2137, C264, C265, C266, C267, C61, C64, C65, C66, C67, C68, C69, C77, C80, C83, C88

PCB CO-LAYOUT

C103, C105, C106, C107, C108, C110, C1208, C125, C1254, C1256, C1267, C128, C144, C145, C146, C151, C152, C153, C154, C159, C160, C161, C162, C170, C173, C2092, C2100, C2101, C2102, C2103, C2104, C2138, C2139, C2140, C2141, C2142, C2143, C2144, C2272, C230, C231, C232, C233, C243, C245, C246, C248, C253, C254, C255, C286, C270, C274, C275, C276, C283, C289, C290, C291, C60202, C62004, C62005

C163, C164, C166, C167, C2087, C2105, C2109, C2110, C2111, C224, C225, C261, C268, C269, C60354, C61428, C62, C63, C89, C91, C96

PCB CO-LAYOUT



MICRO-STAR INT'L CO.,LTD

MS-V389

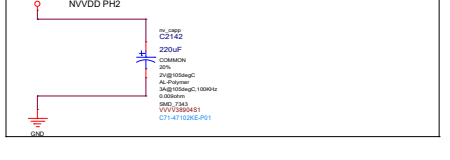
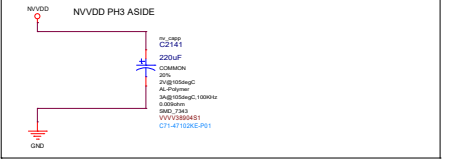
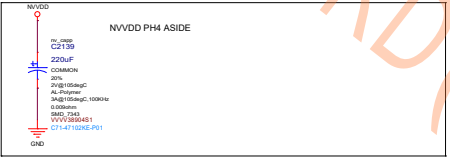
Size	Document Description	Rev
Custom	0060_Colayout_Notes	2.1
Date: Wednesday, July 26, 2020		Sheet 60 of 79



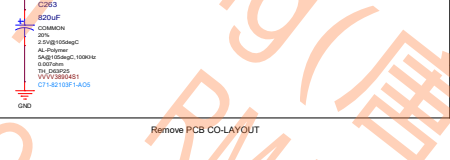
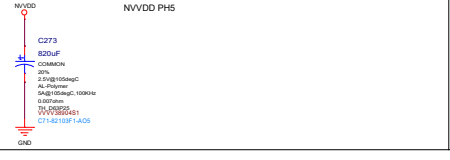
BLANK

	MICRO-STAR INT'L CO.,LTD		
	MS-V389		
	Size	Document Description	Rev
	Custom	BLANK	2.1
Date: Wednesday, July 26, 2020		Sheet 61 of 79	

PS: NVVDD OUTPUT CAP(TOP)



Remove PCB CO-LAYOUT



Remove PCB CO-LAYOUT



REMOVE



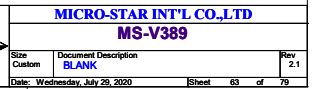
Remove PCB CO-LAYOUT



MICRO-STAR INT'L CO.,LTD		
MS-V389		
Size	Document Description	Rev
Custom	PS: NVVDD OUTPUT CAP(TOP)	2.1
Date: Wednesday, July 26, 2020		
Sheet 82 of 78		

[illegible]

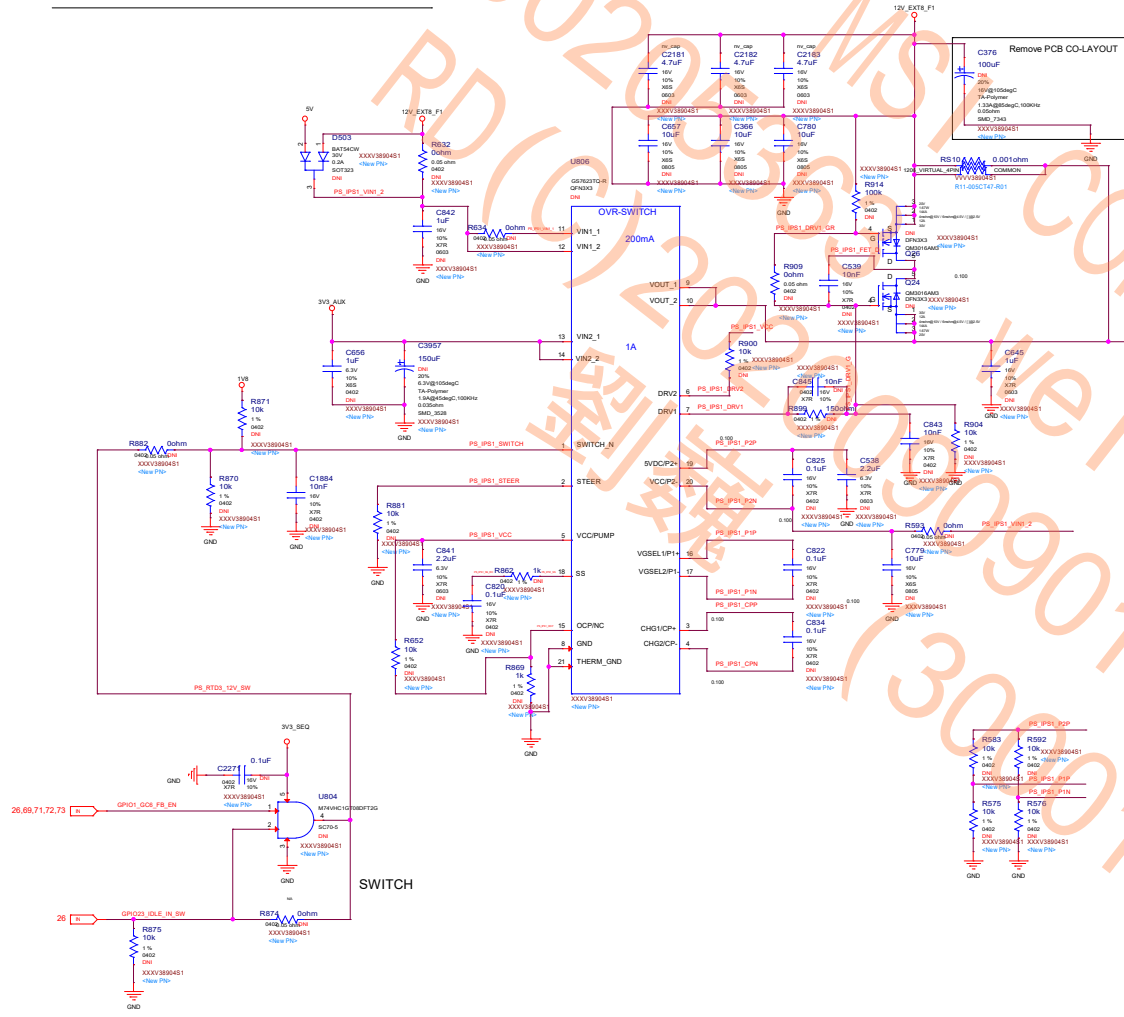
# BLANK



PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

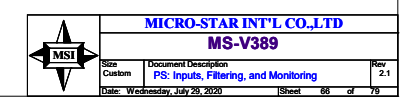
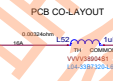
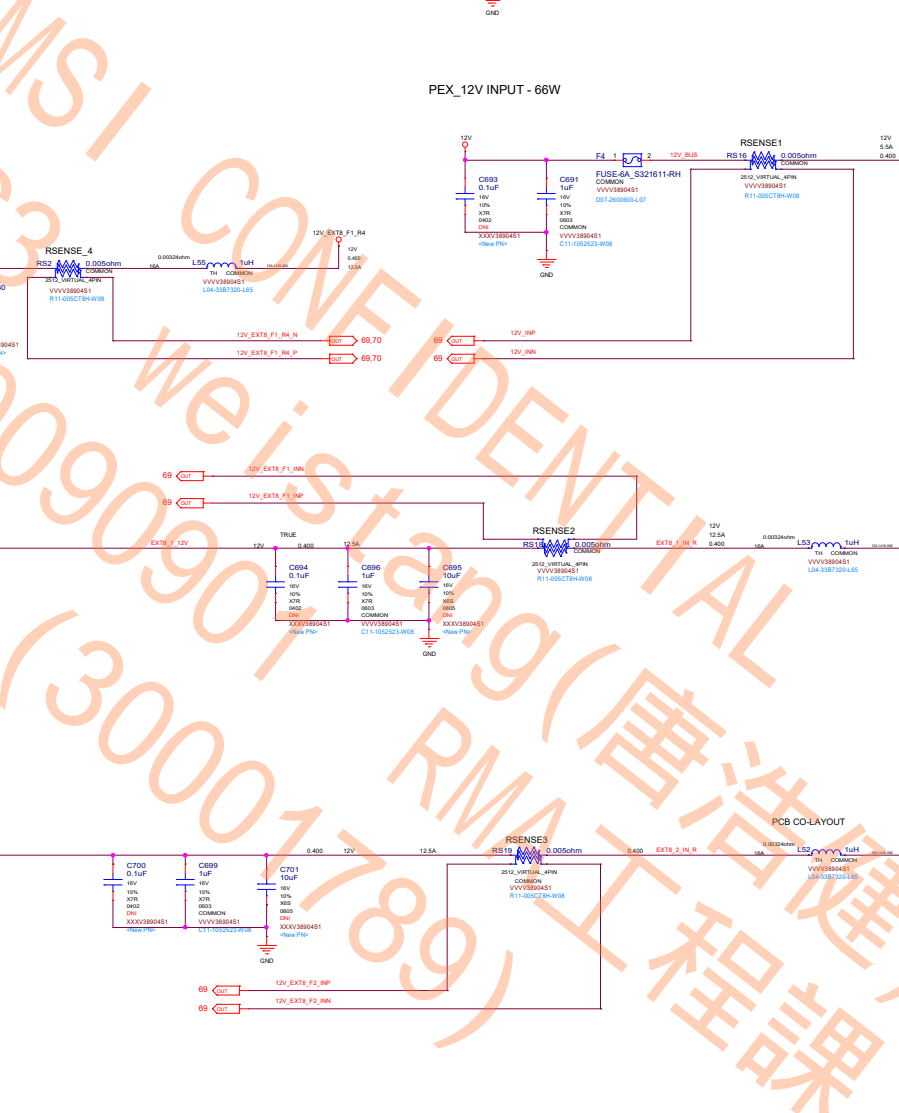
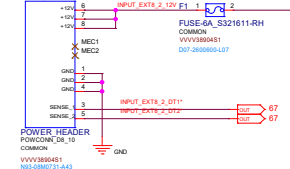
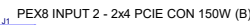
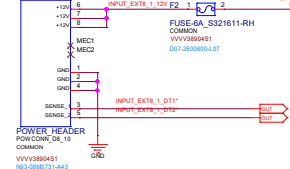
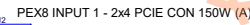
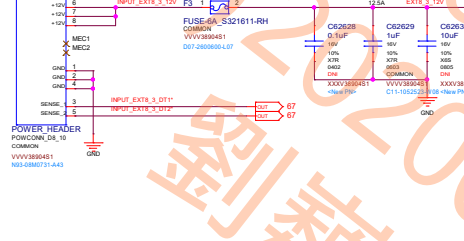
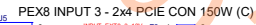
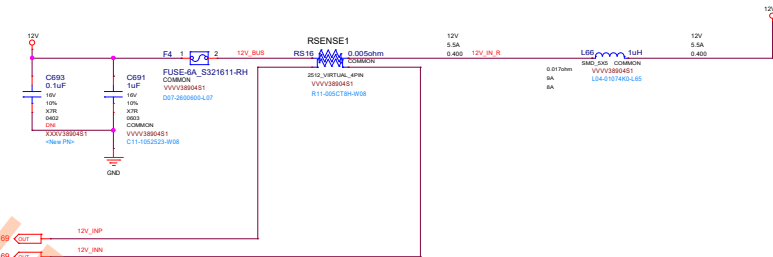
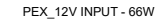
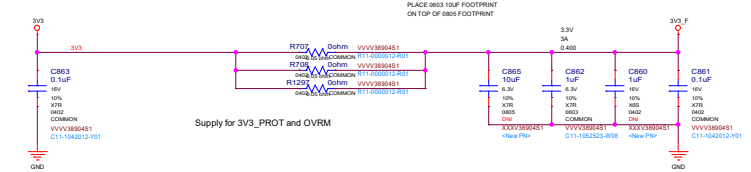
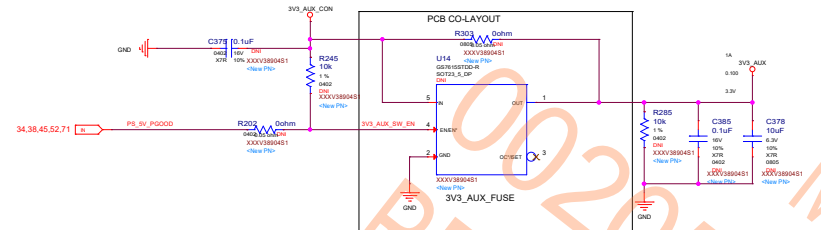
GPI01	GPI023	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



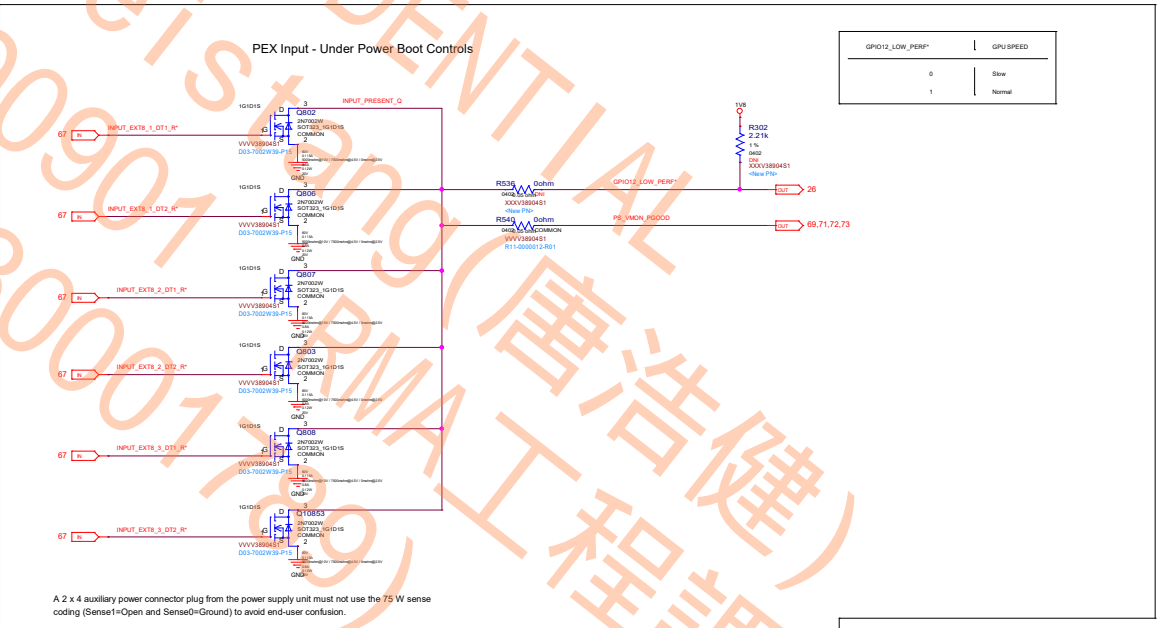
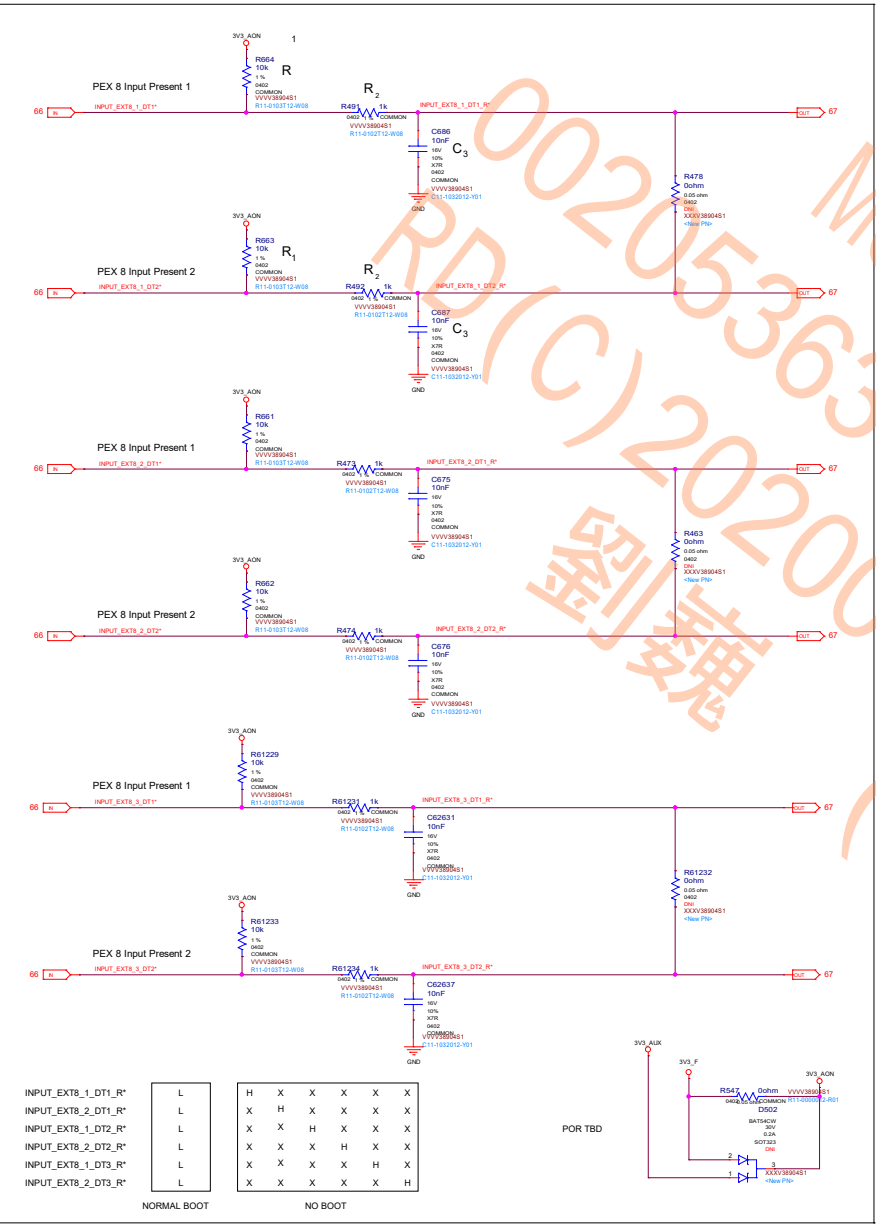
BLANK

	MICRO-STAR INT'L CO.,LTD		
	MS-V389		
	Size	Document Description	Rev
	Custom	BLANK	2.1
Date: Wednesday, July 26, 2020		Sheet 66 of 79	

## PS: Inputs, Filtering, and Monitoring



PS: Hot Unplug Detect





PS: Discrete Steering

12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V\_EXT8\_F1

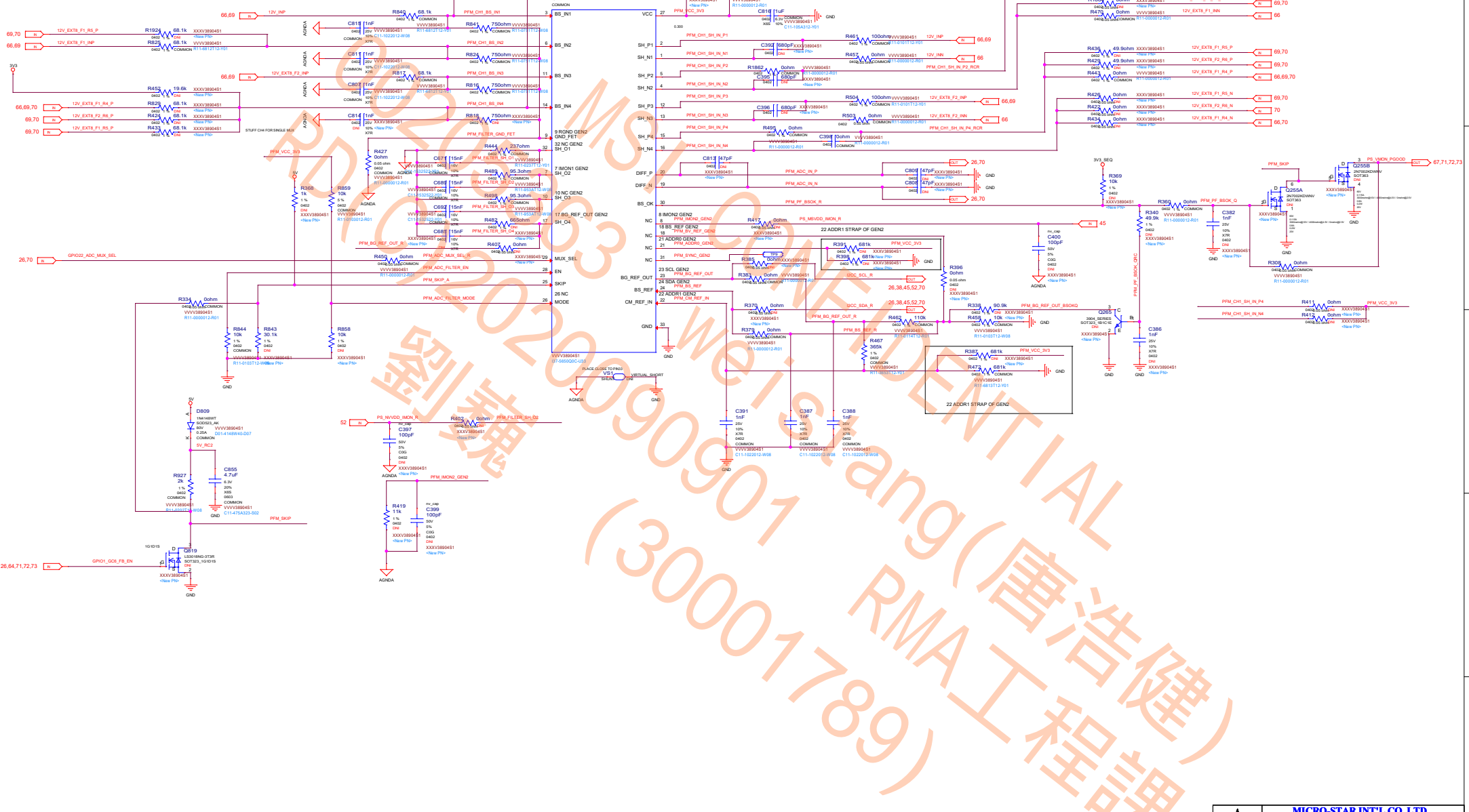
Remove 12V CURRENT STEERING

NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V\_EXT8\_F2

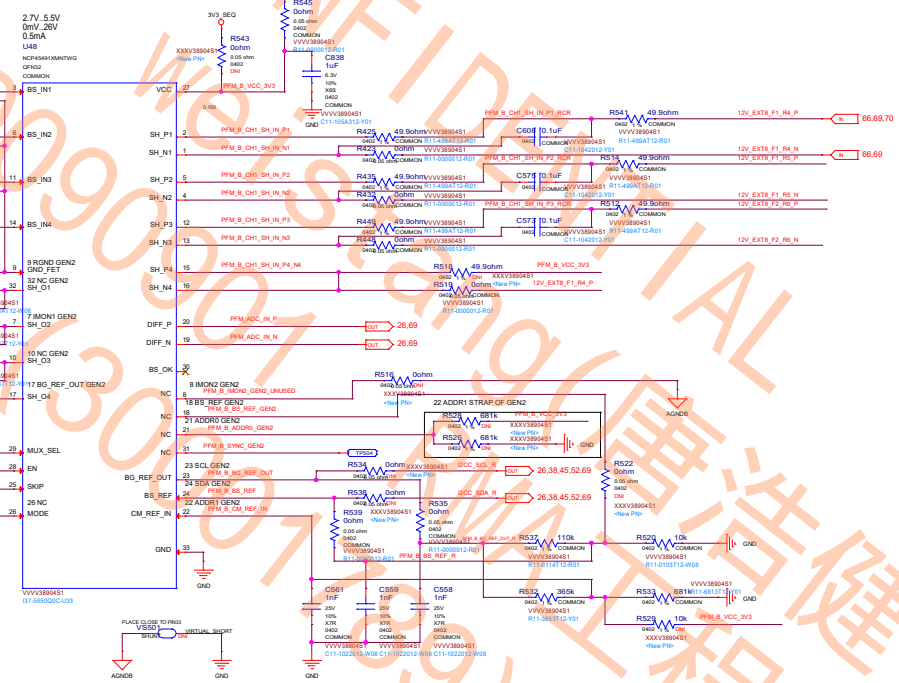
PS: Pre-Filter

Route the trace to PEX Golden Finger



**MICRO-STAR INT'L CO.,LTD**  
**MS-V389**

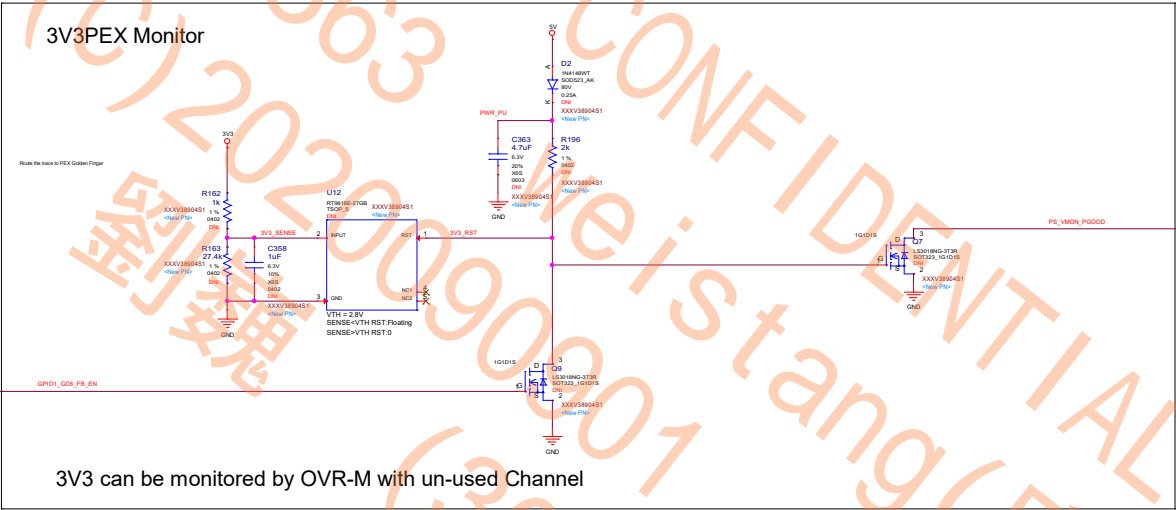
Size Custom	Document Description <b>PS: Pre-Filter</b>	Rev 2.1
Date: Wednesday, July 29, 2020		Sheet 69 of 79



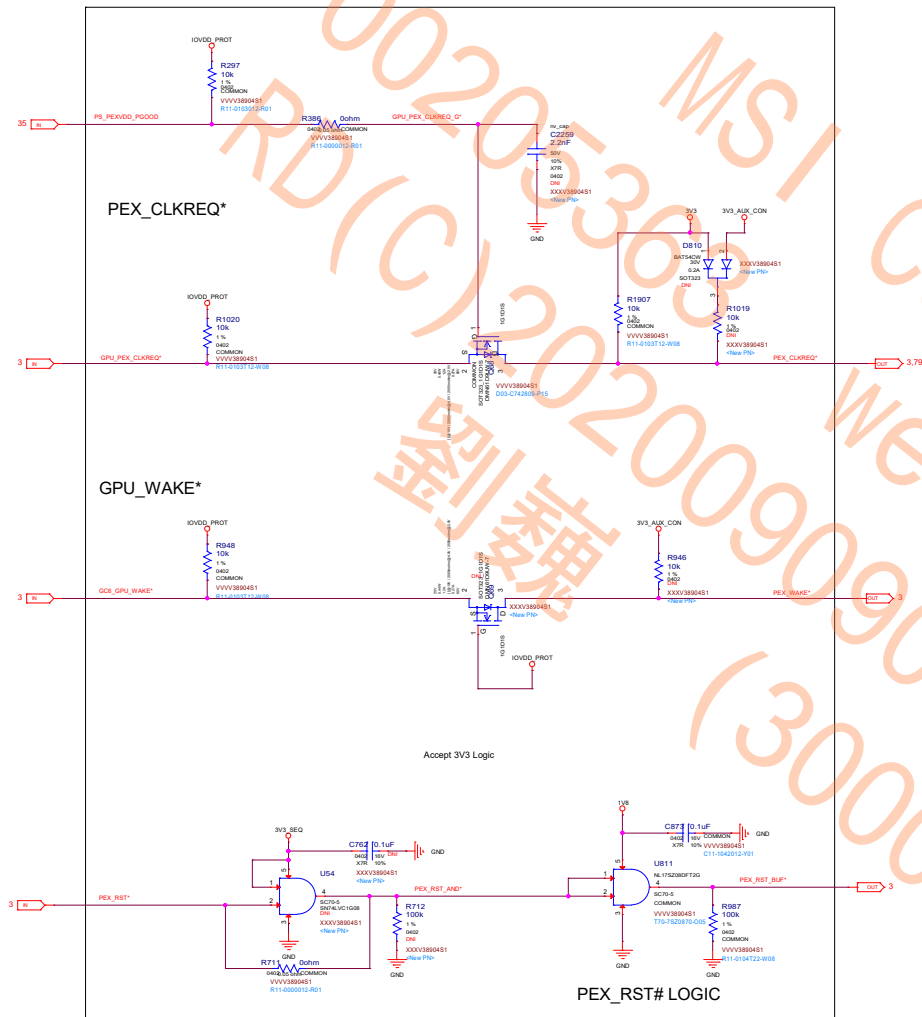




00205363 MSI CONFIDENTIAL  
RD(C) 20200901 Weistang (唐浩健)  
(30001789) RMA工程課



SEQUENCE:MISC



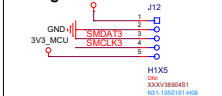




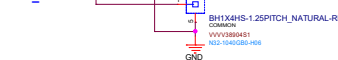
# LED\_CONTROLLER\_IT8295

## Firmware Programming

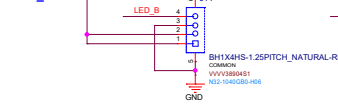
### Debug



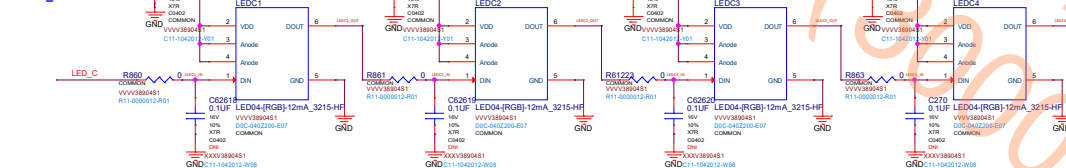
## LED\_A



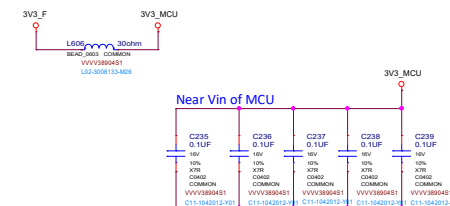
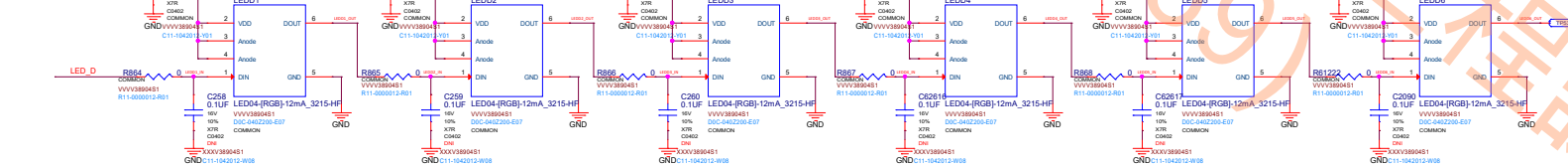
## LED\_B



## LED\_C

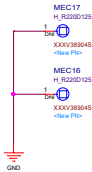


## LED\_D

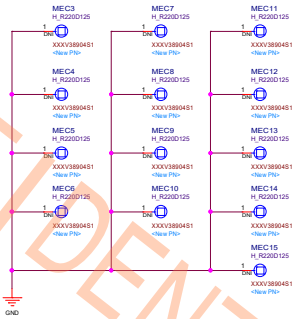
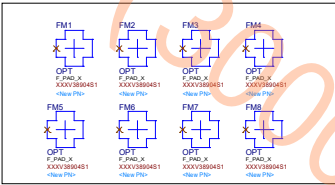
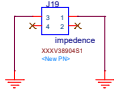
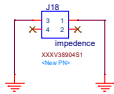


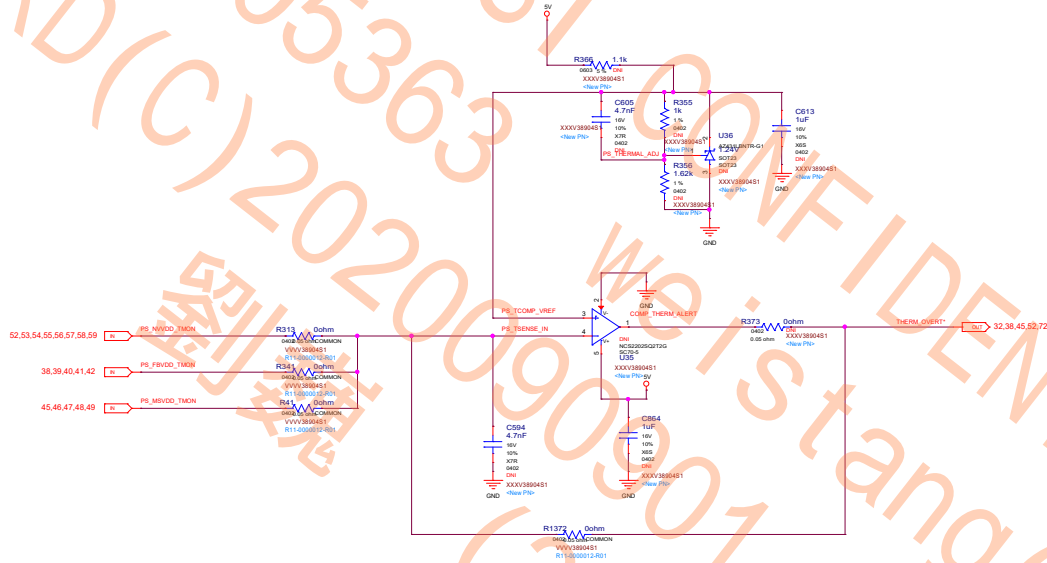
Mechanical: Mounting holes

2 connected mounting pins for Bracket



BACK STIFFENER:





**MICRO-STAR INT'L CO.,LTD**

MS-V389

Size Custom	Document Description <b>VR THERMAL PROTECTION</b>	Rev 2.1
Date: Wednesday, July 29, 2020		Sheet 78 of 79

PCI TERM

